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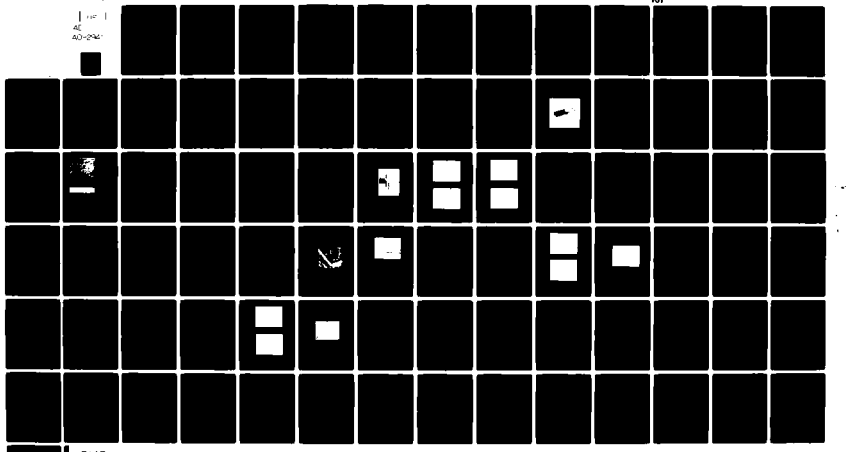

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Research on InGaAs FETs

September 1980

Prepared by:

S. Bandy, S. Hyder, C. Nishimoto and C. Hooper

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The fabrication of Schottky-gate field-effect transistors on InGaAs lattice matched to InP is reported. A higher bandgap interface layer is used to lower the gate leakage to acceptable levels. A technique to deduce the effective saturated electron drift velocity is given which shows over a factor of two higher saturated velocity for InGaAs in comparison to GaAs.

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FOREWORD

The work reported here was supported by the Office of Naval Research, Washington, D.C., under Contract N00014-78-C-0380, and managed by Mr. Max Yoder. The program was aimed at fabrication of FETs on InGaAs lattice matched to InP.

The work was carried out in the Varian Corporate Research Solid State Laboratory. The authors wish to acknowledge the valuable discussion and suggestions of M. Yoder and R. L. Bell.

SUMMARY

Most of the effort for this period was spent in growth of InGaAs lattice matched to InP and subsequent fabrication of FET devices on this material for purposes of evaluation. A capping layer of 1.27-eV InGaAsP for LPE material and InP for VPE material was used to increase the Schottky-barrier height so that acceptable values of gate leakage could be achieved. FETs fabricated on LPE material had InGaAs layers that were too thick to pinch off so that the minimum noise figure could not be measured. However, the LPE FETs were sufficient to determine an effective saturated velocity of 3×10^7 cm/sec for $In_{.53}Ga_{.47}As$ when used as a FET material, which is over a factor of two higher than the 1.3×10^7 cm/sec value typically obtained for GaAs using the same method. Thus, whereas previously the high mobility of LPE $In_{.53}Ga_{.47}As$ was known, it has been confirmed in a quantitative manner that it also has a high saturated velocity when employed as a FET material. Although thinner layers were achieved by VPE, the mobility was lower than for LPE, for some reason as yet undetermined. FETs made on the VPE material, while exhibiting small-signal circuit parameters almost identical to those of GaAs devices having 1.2-1.5 dB minimum noise figures at 8 GHz, were unable to achieve minimum noise figures lower than 9.5 dB at 8 GHz. The problem may be due to gate leakage and is currently being investigated.

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1. INTRODUCTION

1.1 Basis for InGaAs Investigation

Figure 1 shows the position of the Γ, X and L minima for the ternary $In_xGa_{1-x}As$ as a function of x.[1-4] As In is added to GaAs, the bandgap decreases, thus decreasing the Γ effective mass.[5] In addition, the Γ to L energy separation increases so that the threshold for upper valley transfer is increased, assuming that the Γ to X coupling coefficient is relatively independent of composition. This will contribute to shortening the electron transit time through the active gate region, and should lead to improved FET performance over that for GaAs. Although InGaAs has been considered previously as a candidate for an optimum material,[6] an artificial constraint of the intervalley energy separation being larger than the bandgap led to its being considered less desirable than InAsP. GaAs, the best material to date for demonstrated FET performance, does not meet this requirement, and Fig. 1 suggests that InGaAs is an improvement over GaAs with respect to this criterion.

$In_xGa_{1-x}As$ also offers the advantage of differing from GaAs only incrementally, depending upon the value of x, so at least for low values of x the processing technology for GaAs should also be suitable if not better for InGaAs (e.g., the reduced barrier height should reduce the contact resistance of the ohmic contacts). Except for the very high energy values of x, InGaAs has a barrier height advantage over InP. The technique of lattice matching InGaAs to a semi-insulating GaAs substrate by a graded region grown by VPE has been demonstrated on a previous contract,[7] enabling InGaAs to enjoy the benefits of the superior semi-insulating GaAs substrate quality over that of InP, for example.

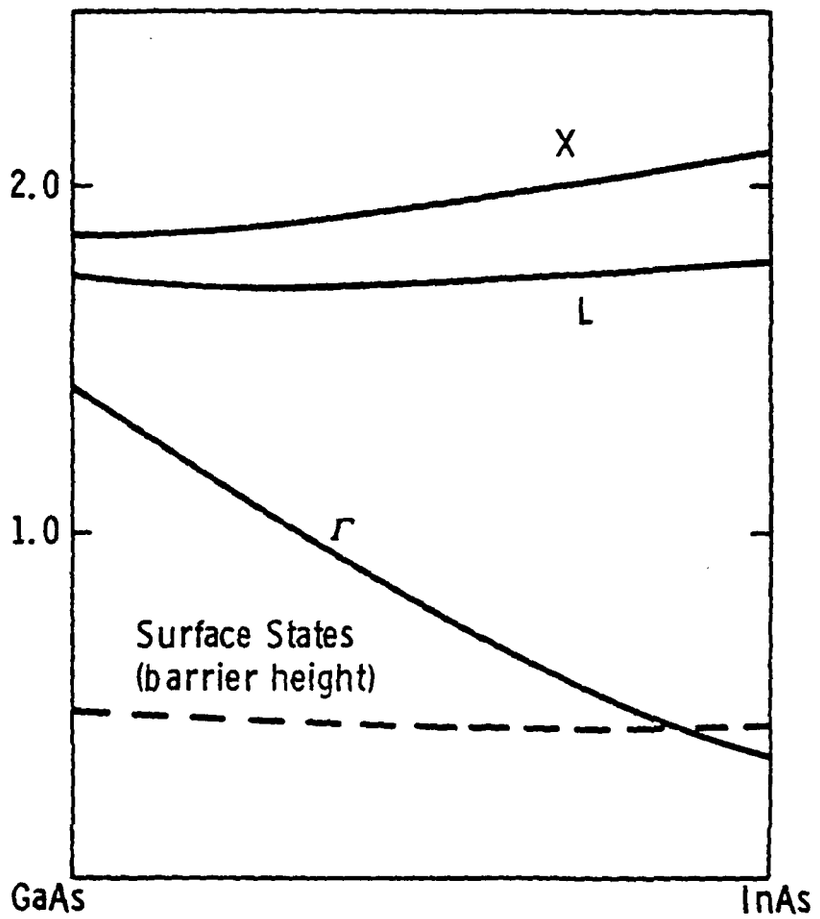


Fig. 1: Schematic of band edges for the InGaAs ternary system.

1.2 Review of Earlier Work

The work on Contract N00014-75-C-0125[7] has shown an effective saturated drift velocity greater than that for GaAs for FETs fabricated using InGaAs. The most positive evidence was obtained from a device run using 34% In grown (as an experiment) on a 2-micron-thick graded buffer layer on an n^+ GaAs substrate (wafer InG 6-3, device run #55). Because of the large values of parasitic capacitance resulting from the n^+ substrate and the thin buffer layer, and because of velocity-degradation at the interface between the active layer and the buffer layer, the rf performance was poor. However, measurements of the static characteristics yielded a saturation drift velocity of 1.8×10^7 cm/sec, or 40% higher than the value for GaAs.

One problem that was encountered was velocity degradation at the active layer-buffer layer interface. It was found that, by growing the last part of the buffer layer in the active layer growth position and lowering the growth rate so that no vapor etch was needed during the transition from buffer to active layer growth, the degradation at the interface could apparently be eliminated, or at least minimized. In spite of velocity degradation at the interface and lower-doped channels, InGaAs was able to match the performance of GaAs, which provided the basis for the expectation that once these problems were eliminated and In percentages above 25% were realized, InGaAs would significantly outperform GaAs.

1.3 Review of Work on the Previous Phase of This Contract

The goal of this contract phase was to grow by VPE active layers of InGaAs having an In percentage of 25% and higher on linearly-graded buffer layers grown on semi-insulating GaAs substrates. Laser annealing and/or ion implantation were to be investigated as a means of

eliminating built-in strain and interface states that give rise to velocity degradation at the active-buffer layer interface. FETs were to be fabricated on this material for the purposes of furthering material evaluation and to compare FET performance with that using GaAs at frequencies above 8 GHz.

It was found that for InGaAs growths with an In percentage at and above 25%, the surface appeared to have what was termed "blue haze", which results from a crosshatch pattern of defects. This blue haze began to appear at around 25% In and became progressively worse as the In percentage was increased. Photoluminescence peaks of the surface layers began broadening at 25% and continued to broaden as the In percentage was increased. Although the blue haze could be polished off, leaving a mirror finish, there was evidence that it was indicative of the nature of the underlying material. FETs fabricated on this material had smaller effective saturated drift velocities than for GaAs, as well as inferior rf performance. Ion implantation of this material was unsuccessful.

Almost all of the effort on this yearly phase of the contract was spent in trying to overcome the "blue haze" problem. It was felt that the problem was not intrinsically associated with the higher In percentages, since the 34% In growth of the previous contract had no such problems. The intention was to duplicate the good growth obtained for that 34% In growth (grown in an earlier version of the reactor using only a 2-micron buffer layer). Many techniques and substrates were tried with limited or no success and it was not until at the very last of this contract phase when an H_2 bypass was installed on the reactor that haze-free surfaces were obtained. Two wafers (InG 45-2 and InG 46-1) having surfaces with a minimum of cross-hatch were grown with the H_2 bypass.

1.4 Goals of This Phase of The Contract

In addition to the fabrication of FETs on wafer InG 46-1 for purposes of evaluation (wafer InG 45-2 was not grown with an active layer) and the possibility of electron-beam annealing the blue-haze wafers to see if the dislocation network can be removed, the majority of the effort is to be expended towards FET fabrication on InGaAs lattice matched to InP to circumvent the problem of achieving good strain- and defect-free material on GaAs for InGaAs growths having an In percentage above 25%.

Other work at Varian has shown that $In_{0.53}Ga_{0.47}As$ alloys can be grown by liquid phase epitaxy, lattice matched on InP, with mobilities in the region of 8000 cm^2/V-sec at 300°K, for dopings of $10^{17}/cm^3$, or nearly twice that for comparable GaAs. (For convenience, the specific lattice-matched $In_{0.53}Ga_{0.47}As$ alloy will be abbreviated as InGaAs in what follows.) The mobility increase is to be expected from the reduced bandgap, but the result indicates that alloy scattering is low in this alloy. Figures 2 and 3 show plots for the entire range of quaternaries from InP to InGaAs of mobility, Schottky-barrier height, and estimated satellite valley spacing (Γ - L; X appears to lie higher than L for the entire range of alloys matched to InP). The high mobility of InGaAs is coupled with a large (1.0 eV) gap to the nearest conduction band satellite valley. This implies that under the moderately high fields found in a microwave FET, considerable velocities can be reached in the central Γ valley before transfer to the L satellites sets in. To achieve this in GaAs requires the use of strong "overshoot" effects, i.e. gate lengths in the region of 0.1 μm.[8] However, the overshoot effect should be seen for more conventional dimensions (0.5 to 1 micron) in InGaAs. A transition to still shorter gate lengths using InGaAs should, of course, maintain the advantage over GaAs.

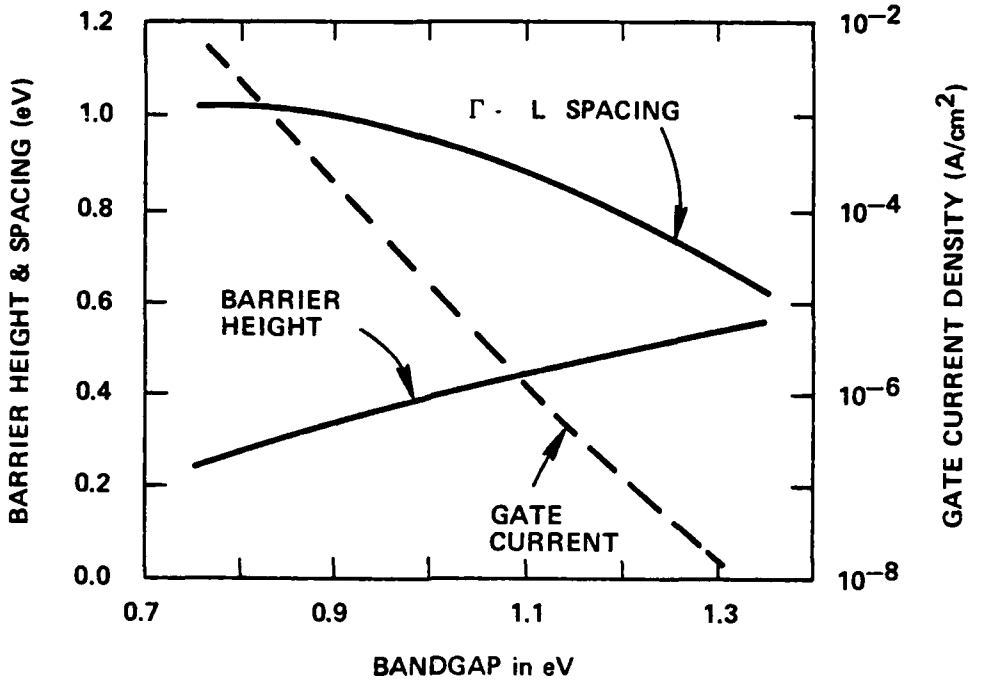


FIGURE 2
Quaternary barrier height, Γ-L spacing, and leakage current as a function of bandgap.

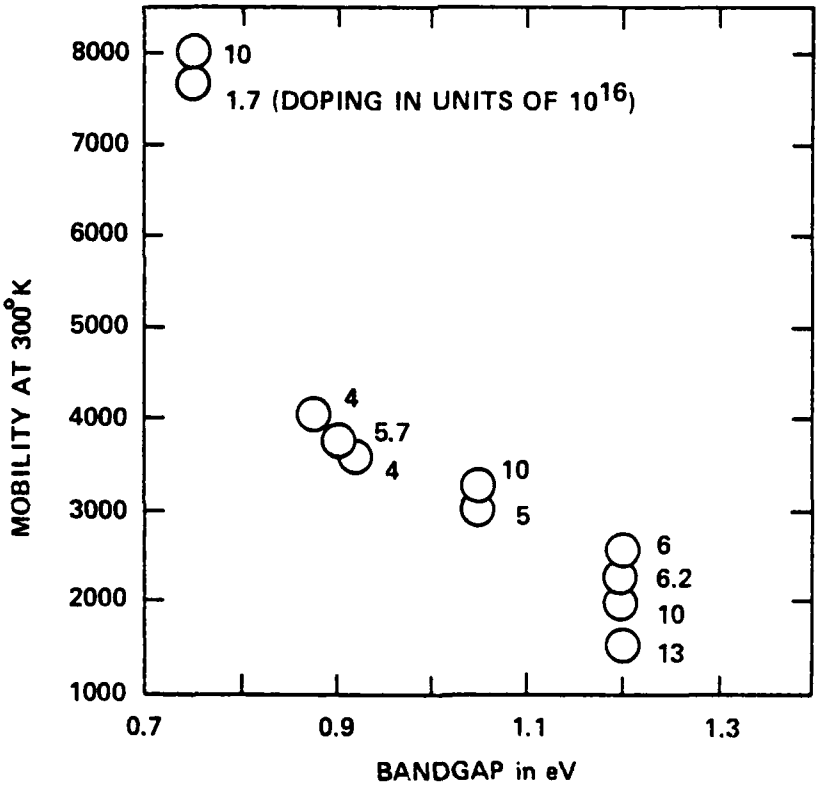


FIGURE 3
Experimental mobilities as a function of quaternary bandgap.

Some concern remains regarding the possibility of low-field avalanching in a material where the bandgap (0.73 eV at 300°K) is less than the satellite valley spacing (about 1.0 eV for Γ - L). However, this does not appear to be troublesome. Experiments in this laboratory with high-field bias-assisted photoemission from InGaAs[9] show that fields adequate for Γ - L transfer can be applied without avalanching. Once transfer to the heavy-mass L and X-band edges is achieved, a very large further increase in field is necessary to produce significant electron-hole pair generation. Fields used in the photoemission experiments[9] are of the order of 30 kV/cm. Qualitatively, InGaAs would be expected to behave somewhat like GaSb, which has a direct gap of about the same magnitude. Computations of Hauser[10] show that fields of about 200 kV/cm would be required in 10^{17}-doped GaSb to cause avalanching.

As can be seen from Fig. 2, the low Schottky-barrier height on InGaAs leads to very high gate current densities, and indeed initial attempts to fabricate MESFETs directly on this alloy at Varian have led to shorted gates. At the same time, attempts to use oxides or other insulators on III-V compounds have met with very limited success, due to high densities of interface states and instabilities of the insulators themselves. Accordingly, it is proposed to make use of lattice-matched InP or the higher bandgap InGaAsP quaternaries:

(1) in n-type form to provide the higher Schottky barrier (Figs. 4a and 4b), or

(2) in p-form to provide a junction FET (Fig. 4c).

In either case, the channel electrons flow in the low-bandgap high-mobility material, while the adjacent high-bandgap material is depleted; hence, the low mobility of the depleted material is of no consequence. Figure 4b has an advantage over 4a in that ohmic source and drain contacts

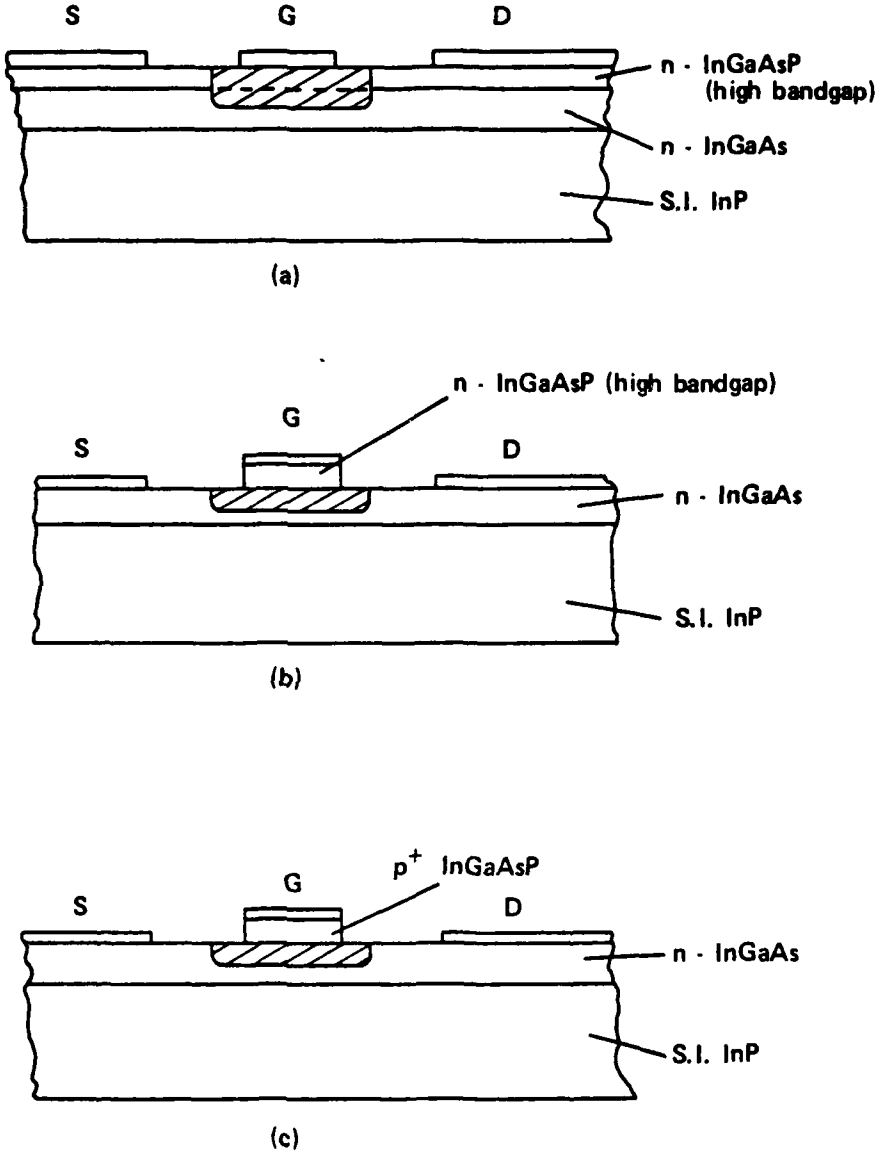


Figure 4 Possible Gate Configurations for InGaAs FET.

to the InGaAs should be easier. This may not be a very significant advantage, considering the extra complexity. The junction FET of Fig. 4c has the advantage of a still higher barrier height, if diffusion of the acceptor species in the p gate can be adequately controlled. A low-resistance gate contact can be developed using Be implantation.

Initial work would use LPE growth of the layers, which has given the highest mobilities in InGaAs. Experimentally, it has been found easier to grow high-bandgap quaternaries on InGaAs than pure InP on InGaAs. In all cases, very thin layers are needed, especially for submicron devices, providing strong motivation for development of complete vapor phase growth of these systems. Vapor phase growth of InGaAs on InP has not yet demonstrated the high mobilities of LPE. However, this work is in a very preliminary stage, and it is proposed to devote some effort to improving the state of VPE of InGaAs grown on InP for this application. Ultimately, MBE may be applicable to the proposed structures. However, MBE technology has far to go in this area, and meanwhile feasibility investigations can be carried out using more conventional growth techniques. The use of different materials for gate and channel also suggests the applications of selective etching for submicron self-aligned structures.[11]

2. InGaAs MATERIAL GROWTH

$In_{.53}Ga_{.47}As$ lattice matched to (100)-oriented InP substrate can be grown both by liquid phase epitaxy[12] and vapor phase epitaxy.[13] VPE growth is quite suitable for submicron layer growths necessary for FET structures; but for growth by liquid phase epitaxy, the step-cooling technique from a critically-saturated melt has to be used for reasonably uniform thin layer growths and adequate thickness control. It is desirable to have as large a Schottky-barrier height as possible for MESFET fabrication, but n-$In_{.53}Ga_{.47}As$ has a barrier energy of only about 0.3 eV. This disadvantage can, however, be overcome by growing a material with a larger barrier height on top of the InGaAs active layer. InP or a high-bandgap quaternary layer grown lattice matched to InGaAs can be this layer that will have a barrier height of about 0.5 eV.

2.1 LPE Growth

Attempted growth of InP on InGaAs by LPE results in a rapid dissolution of InP, as the P component is absent from the InGaAs inner layer, especially if the InGaAs/InP has to be grown with limited supercooling. However, a high-bandgap quaternary InGaAsP can be grown by supercooling technique on $In_{.53}Ga_{.47}As$. On the other hand, InP on InGaAs presents no problem by VPE growth. LPE growth of InGaAs is fairly well established at present, whereas the technology of $In_{.53}Ga_{.47}As$ growths by the hydride process is comparatively new.

A 1.27-eV Q/InGaAs/InP structure was grown by liquid phase epitaxy utilizing the conventional slider boat technique and using the step-cooling method of growth from a supersaturated melt. Table I gives the melt composition used for InGaAs and 1.27-eV quaternary growths. Indium metal was prebaked at 700°C in Pd-diffused H_2 flow for about 72 hours. The GaAs, InP, and InAs were best-available, undoped single-

TABLE I

Material	In	GaAs	InAs	P	Sn
InGaAs	3.26137	0.121366	0.220275	---	.0036
1.27-eV Q	3.31889	0.003825	0.0613236	0.02672	.00736

crystal material. The InGaAs melt was also baked at 650°C for 72 hours without a graphite plug on the melt. A graphite plug was, however, used after the bakeout and during growths.

Figure 5 shows the arrangement of melts in the graphite slider for the growth of InGaAsP/ InGaAs heterojunction FET structure. The substrate was Fe-doped (100)-oriented *InP* polished in Br-methanol, etched in 4:1:1 H_2SO_4:H_2O_2:H_2O for 1 min. to remove any oxides and then etched further for 2 min. in a 17:1:300 solution of HBr:Br:H_2O. The substrates were protected from thermal decomposition by use of a Sn-P basket[14] which supplied an over-pressure of P. The InGaAs melt was kept upstream of the Sn-P basket to avoid any contamination of P from the Sn-P basket.

For growth, the heat-pipe-lined furnace was rolled onto the reactor tube containing the graphite boat and the temperature raised to 10°C above the saturation temperature to 660°C to homogenize the melt. After a soak period of about 40 min., the temperature was lowered at a rate of about 1-1.6°C per minute to 640°C, a level 10°C below the saturation temperature. After a 10-min. temperature stabilization period at the growth temperature, the slider was moved to bring the InGaAs melt

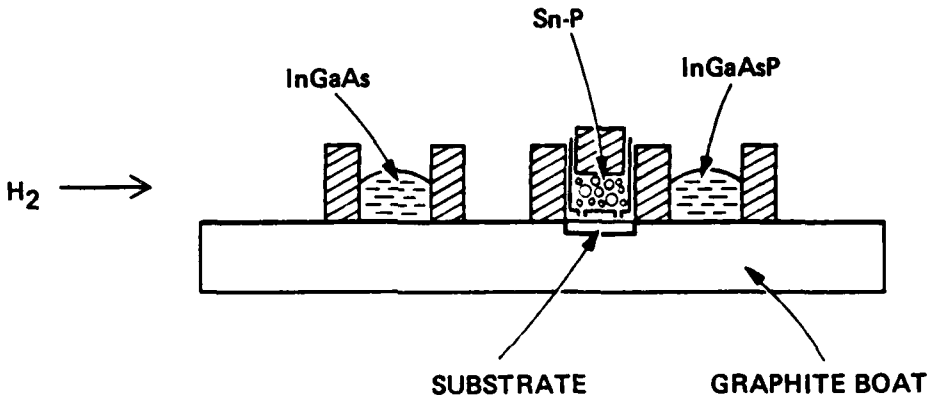


Fig. 5 Schematic of melt set-up used for LPE growth of InGaAsP/InGaAs layers.

over the substrate; and after the desired time of growth, the quaternary melt was brought in contact with the substrate for the second layer growth. The typical times of growth on each melt were about 1 sec. and the expected total thickness was about 3000 Å.

The carrier concentration and mobilities in the material were determined separately in trial runs by van der Pauw analysis, and lattice matching was determined by X-ray diffraction. Bandgap measurements on FET layers were made by photoluminescence at 77°K, using an argon ion laser. Carrier concentration on the actual FET layer was measured by C-V profiling at 77°K. The best mobility obtained in InGaAs (Sn) was 7990 cm^2/V-sec for a doping level of $1.17 \times 10^{17} cm^{-3}$. Figure 6 shows the photoluminescence spectra of InGaAs and quaternary InGaAsP obtained from a double-layer FET structure. The InGaAs photoluminescence was recorded with a PbS detector using a 1.4 μm grating, whereas the quaternary photoluminescence was recorded by an S-1 photocathode using a 7500 Å grating.

2.2 VPE Growth

The VPE technique has several advantages, such as good surface morphology, better layer thickness and doping profile control, sharper heterojunction interfaces, ease of composition change and possibility of high yields and low background dopings. Also, fabrication of heterojunctions -- like InP/InGaAs/InP, for example -- which are difficult with LPE, present practically no problem with VPE growth, by which means submicron InP/InGaAs layers can be grown alternately. The problem with VPE, at present, is of low mobilities and is related to the inadequate purity of commercially-available source gases and the corrosive effect of HCl on commercially-available cylinders.

The experimental reactor system that is used for growth of InGaAs is shown in Fig. 7. The reactor tube is 40-mm spectrosil quartz

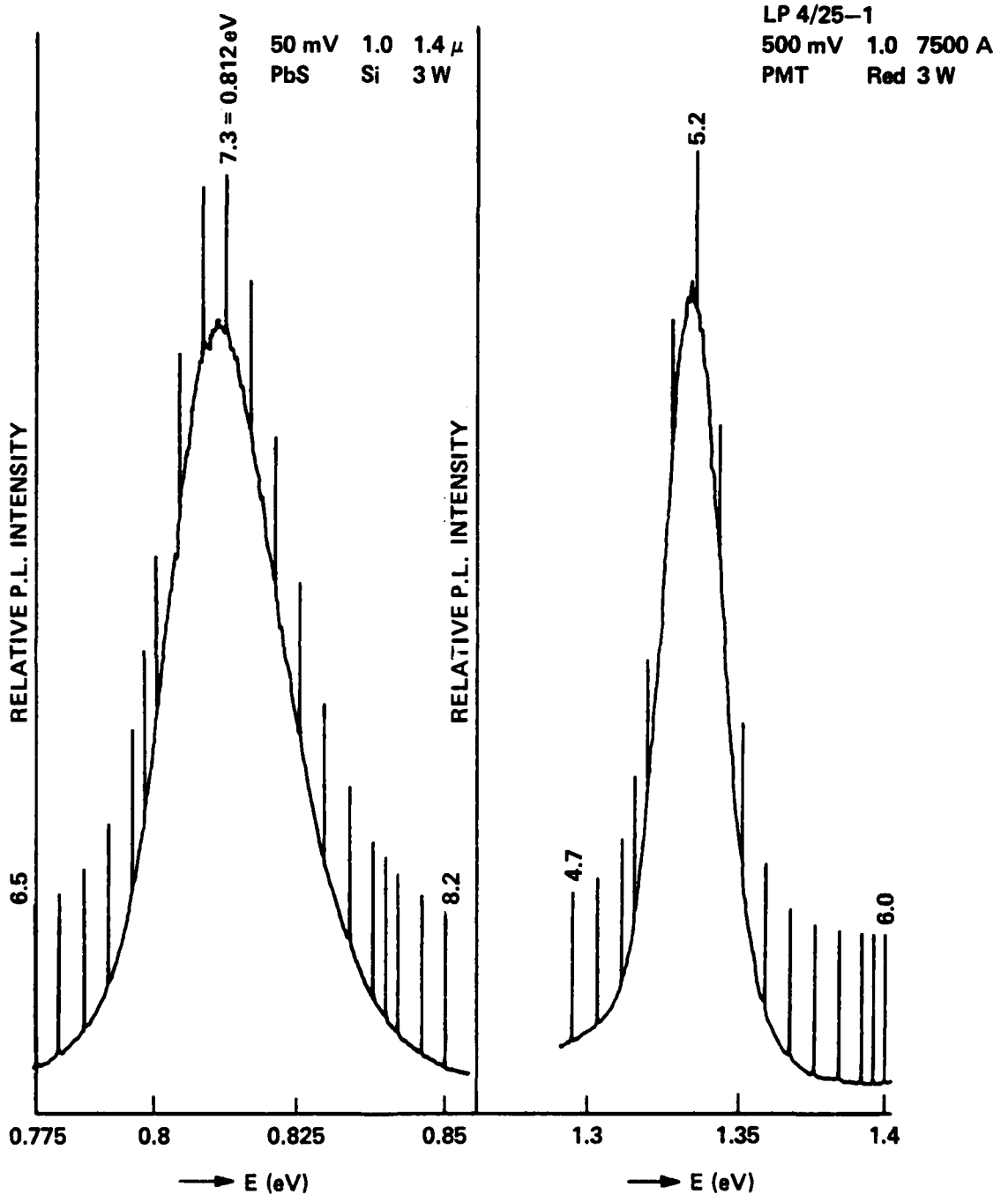


Fig. 6 Photoluminescence spectra of a thin layer of InGaAsP on InGaAs lattice matched to InP substrate.

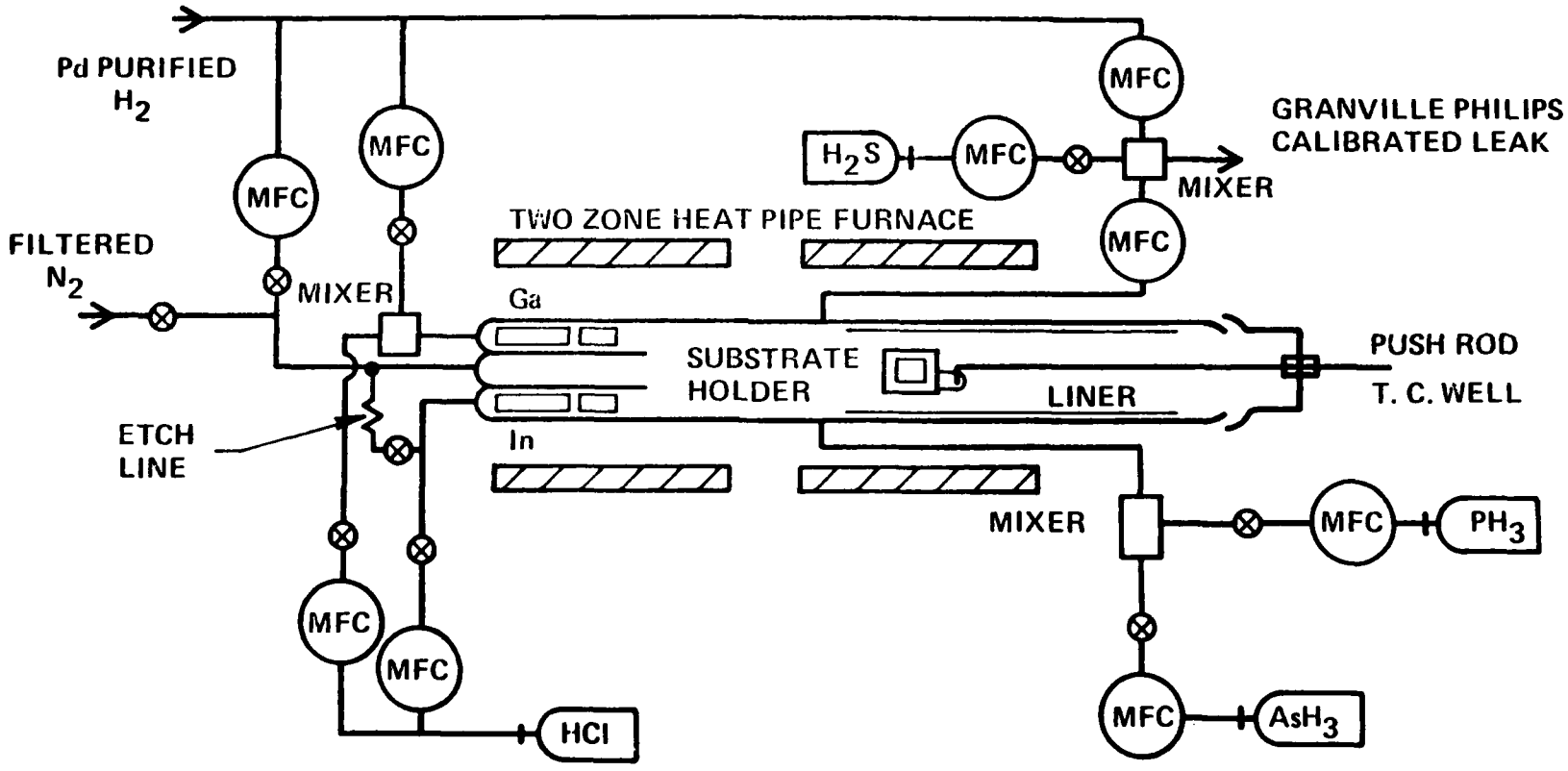


Fig. 7 Schematic diagram of the quaternary $In_{1-x}Ga_xAs_yP_{1-y}$ VPE growth system.

and about 4 feet long. Two source chambers separate Ga and In, which are placed in about 10-cm long spectrosil boats exposing a surface area of about 16 cm^2 to the incoming HCl flow. The sources are kept at 850°C and the growth area temperature is maintained around 688°C. A two-zone heat-pipe-lined resistance-heated furnace is used and the AsH_3 and PH_3 ports are placed in the lower temperature region about 8 cm upstream of the position at which the substrate holder is placed for growth. The substrate holder is of special design shown in Fig. 8, and protects the substrates from any thermal decomposition prior to growth. The holder consists essentially of two flat quartz plates. The bottom plate is fused to a quartz tube cut in half and contains an ultrasonically-cut recess in which the substrate is placed. The top plate, operated by a push rod, is free to slide on and off the substrate recess in channels fabricated with flat quartz strips. Although recently others have adopted the use of a slider boat,[24] Varian has used this technique for several years,[13,25,26] being originally developed for the growth of InGaAs/InP hybrid photocathodes[27] to avoid etchback and to allow time for composition changes and HCl saturation of the In source. The substrate temperature is recorded by a platinum-platinum/rhodium thermocouple placed in a second quartz tube held underneath the substrate plate and also holds the substrate holder in any place in the reactor.

The gas-handling system is all stainless steel, and calibrated Tylan mass flow connectors are used to control all the gas flows. The AsH_3, PH_3 and HCl are all 10% concentration in H_2 and are normally 5-9's pure (<10-ppm total impurities). The indium is typically 6-9's pure and the gallium is of 7-9's purity. The substrate wafers are chemi-mechanically polished in 1% bromine methanol solution. Substrate preparation before growth involves degreasing and DI-water rinse, followed by a 4:1:1 (H_2SO_4:H_2O:H_2O) etch and a 17:1:300 (HBr:Br:H_2O) solution etch. This is followed by a DI rinse and a boil in IPA. The wafers are then blown dry with N_2 and loaded directly into the slider boat holder.

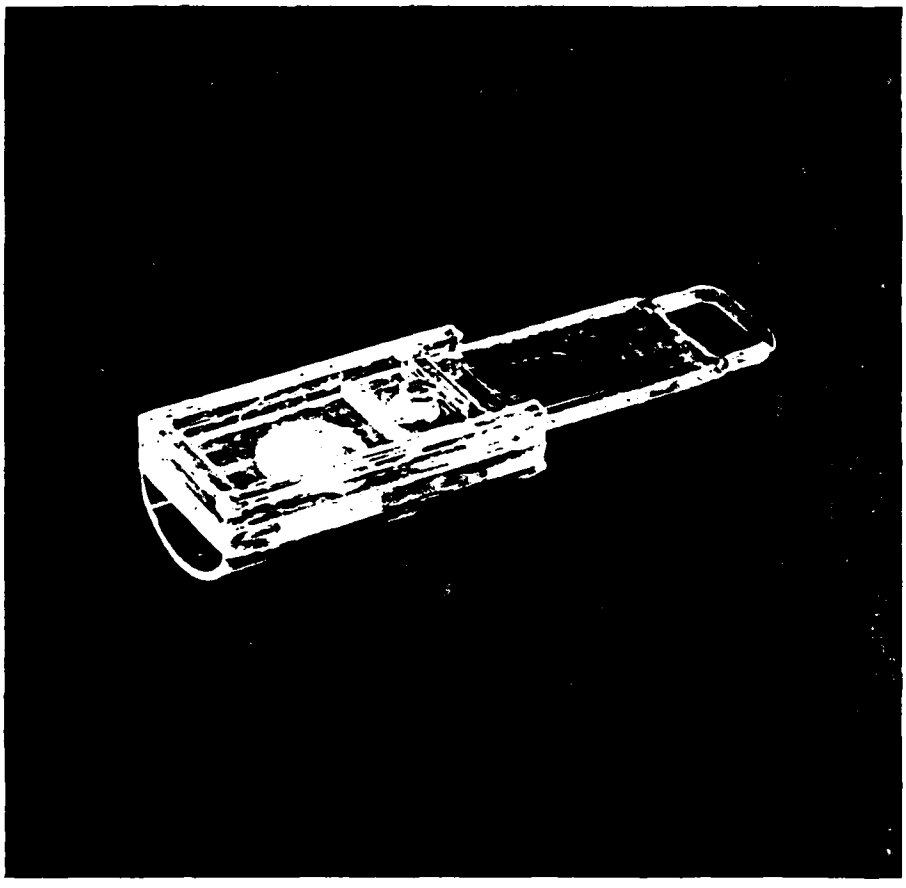


Figure 8 Photograph of the "slider boat" substrate holder.

Figure 9 shows the Ga/In + Ga)(HCl) flow ratio against temperature of growth reported earlier by Hyder et al.[13] for different Ga-HCl flows. For a fixed growth temperature, the Ga/(In + Ga) HCl ratio is seen to increase with Ga-HCl. The growth curves for InGaAs shown in Fig. 9 were generated using a $\frac{InCl + GaCl}{AsH_3}$ flow ratio of 3:1, as this flow ratio appeared to yield the best mobilities and least extraneous wall deposits for the fixed condition of 1100 cc/min bypass H_2 flow. Figure 10 shows a plot of variation of In-HCl flow with AsH_3 flow for 6 cc of Ga-HCl for InGaAs growth at 688°C. The top curve in the same figure shows the effect of AsH_3 flow increase on the $\frac{Ga}{In+Ga}$ ratio. For the growth of InGaP, Enstrom et al.[15] observed that an increase of PH_3 in the system promoted InP deposition, while an excess of HCl suppressed the InP content. A similar effect appears to be occurring in InGaAs growth here, where an increase in AsH_3 in the system had to be compensated for, by increasing the In-HCl flow to obtain lattice-matched growth.

Some attempts were also made to check the effect of lowering the source temperature from the normally-used 850°C to as low as 780°C, keeping the growth temperature at 688°C. No marked effect on the carrier concentration was observed; however, the extraneous wall deposits were reduced and the Ga/In HCl ratio for a fixed Ga-HCl flow increased due to incomplete reaction and lower solubility of InCl in the In source.

Practical device structures generally require multiple layer growths. In an open substrate system, the substrate has to be removed from the growth zone into a protective chamber, while the gas flows are appropriately changed for the next growth. Alternatively, a multiple barrel reactor system can be used, where each barrel is set for one particular growth and the substrate switched from one barrel to another. The present system alleviates the need for such modifications, as the

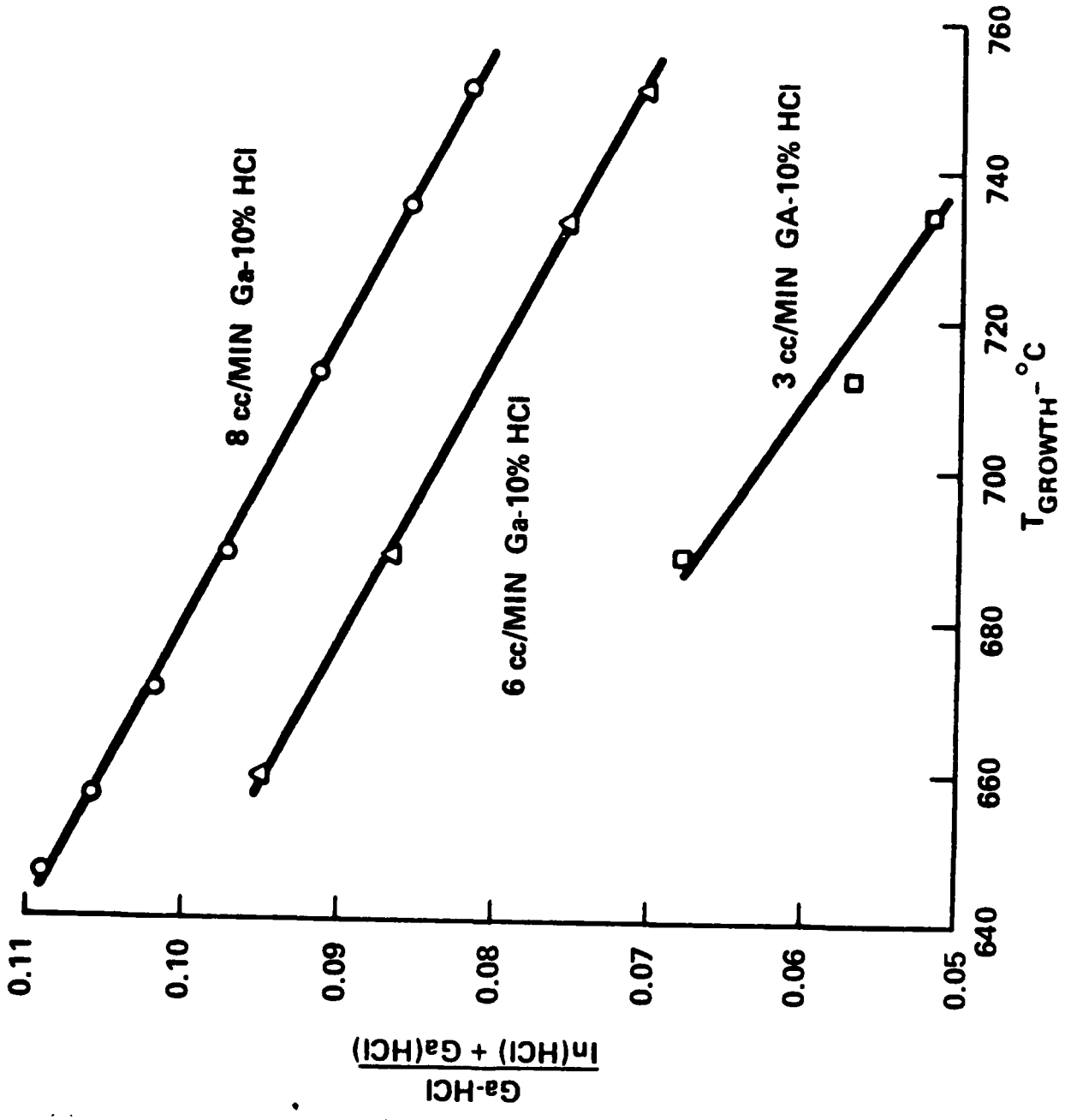


Fig. 9 Change of Ga/(In + Ga)HCl flow ratio with growth temperature for growth of InGaAs lattice matched to InP for Ga-HCl flows.

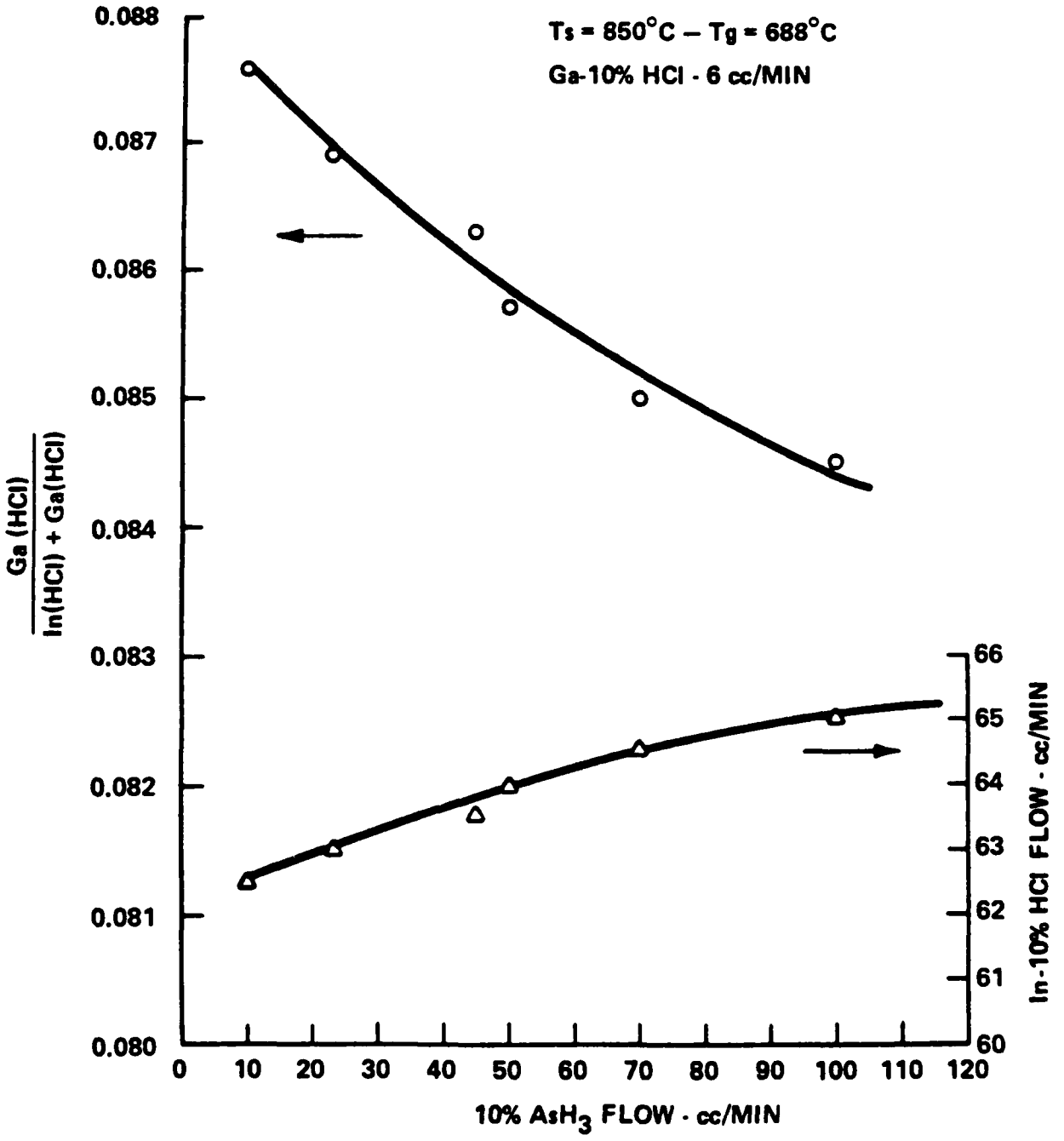


Fig. 10 Effect of AsH_3 flow on In-HCl flow and Ga/(Ga + In) flow ratios for a fixed Ga-HCl flow of 6 cc/min.

substrate is kept in a slider boat which can be conveniently closed during alterations of the gas flows for subsequent growths. Sometimes an extraneous nucleation from a previous growth can interfere with the growth rate integrity and composition of the subsequent layer, and hence an etchback of the reactor in between layers becomes necessary.

Figure 11 shows the scheme used presently for multilayer growths. The substrate is initially kept in position 1 with the slider closed during thermal equilibration and saturation. For growths, the substrate is pushed in position 2 and the slider is operated. After the desired growth period, the slider is closed again and the substrate holder is pushed in position 3. The reactor is etched by diverting the HCl flow through the AsH_3/PH_3 port between positions 2 and 3. The flows are then adjusted for the next growth and the substrate holder is pushed back to position 2 for the growth of the subsequent layer.

Figure 12 shows the surface, and also the cleaved and etched section of an InP/InGaAs/InP structure grown using the procedure described. The InGaAs layer is about 7μm thick and the InP cap layer is about 2 μm in thickness. Use of closed slider boat substrate holder also makes it convenient to reproducibly grow submicron layers, and for a few thin layers, the etchback step can also be eliminated. Figure 13 shows the photoluminescence spectra using an argon ion laser of an InP/InGaAs/InP structure grown in a slider boat holder. The InGaAs layer was 1000 Å thick, the InP contact layer was 1500 Å, and both layers were doped n-type to about $1 \times 10^{17} cm^{-3}$ using H_2S as a dopant. The InP surface photoluminescence spectrum is taken with a 7500 Å grating using an S-1 photomultiplier as a detector, while the InGaAs PL is taken using a 1.4 μm grating and PBS detector. The substrate PL cannot be observed through the low-bandgap InGaAs, but InP top layer is transparent to the InGaAs photoluminescence.

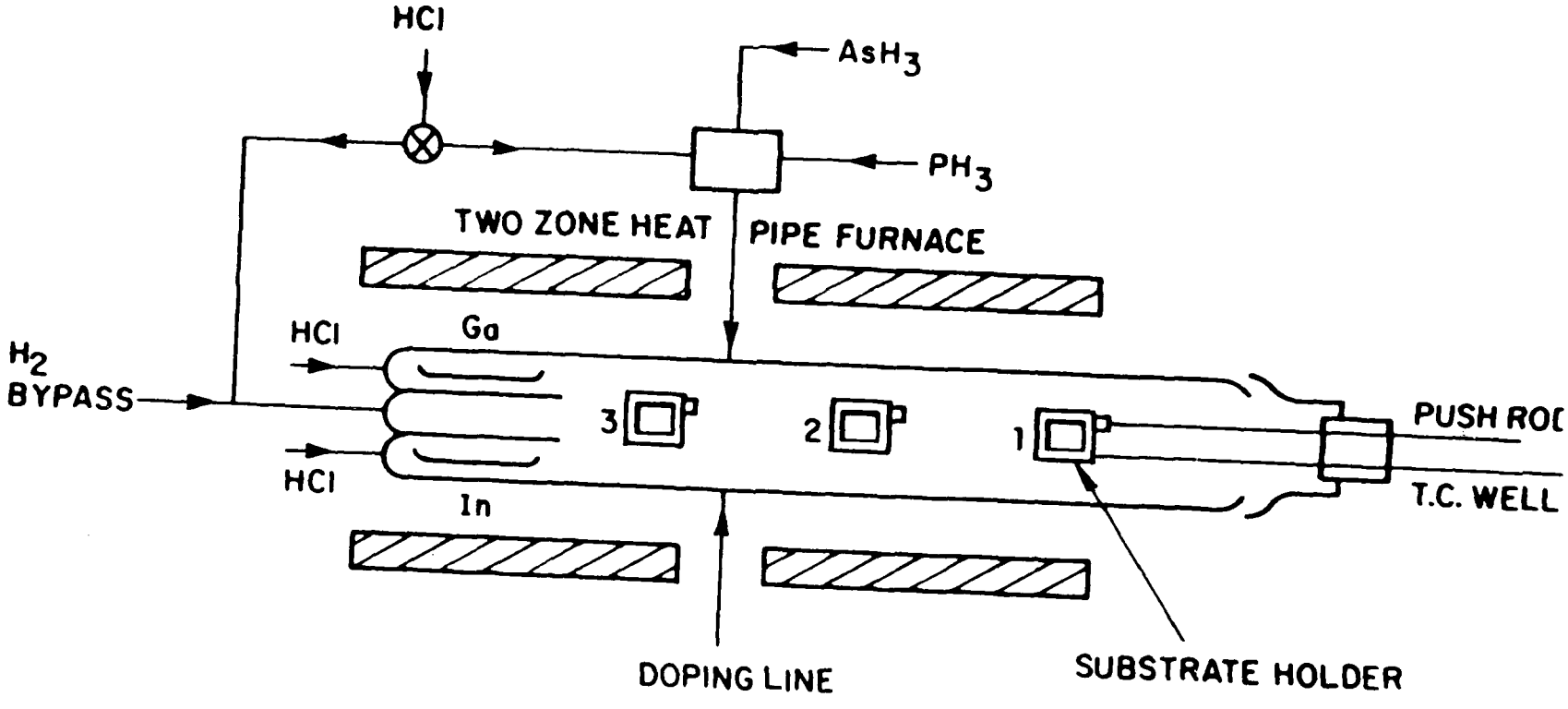


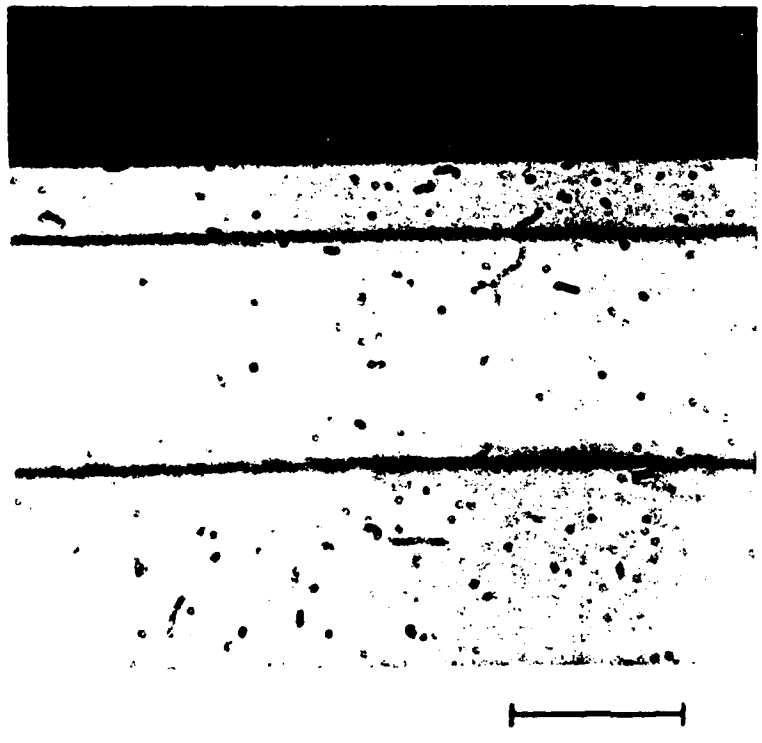
Figure 11 Schematic diagram of reactor and substrate holder positions for multilayer growth

(a)

180 μ

Fig. 12(a) Optical surface micrograph of $In_{.53}Ga_{.47}As$ growth on (100) InP substrates.

(b)



P-InP $3 \times 10^{18} cm^{-3}$

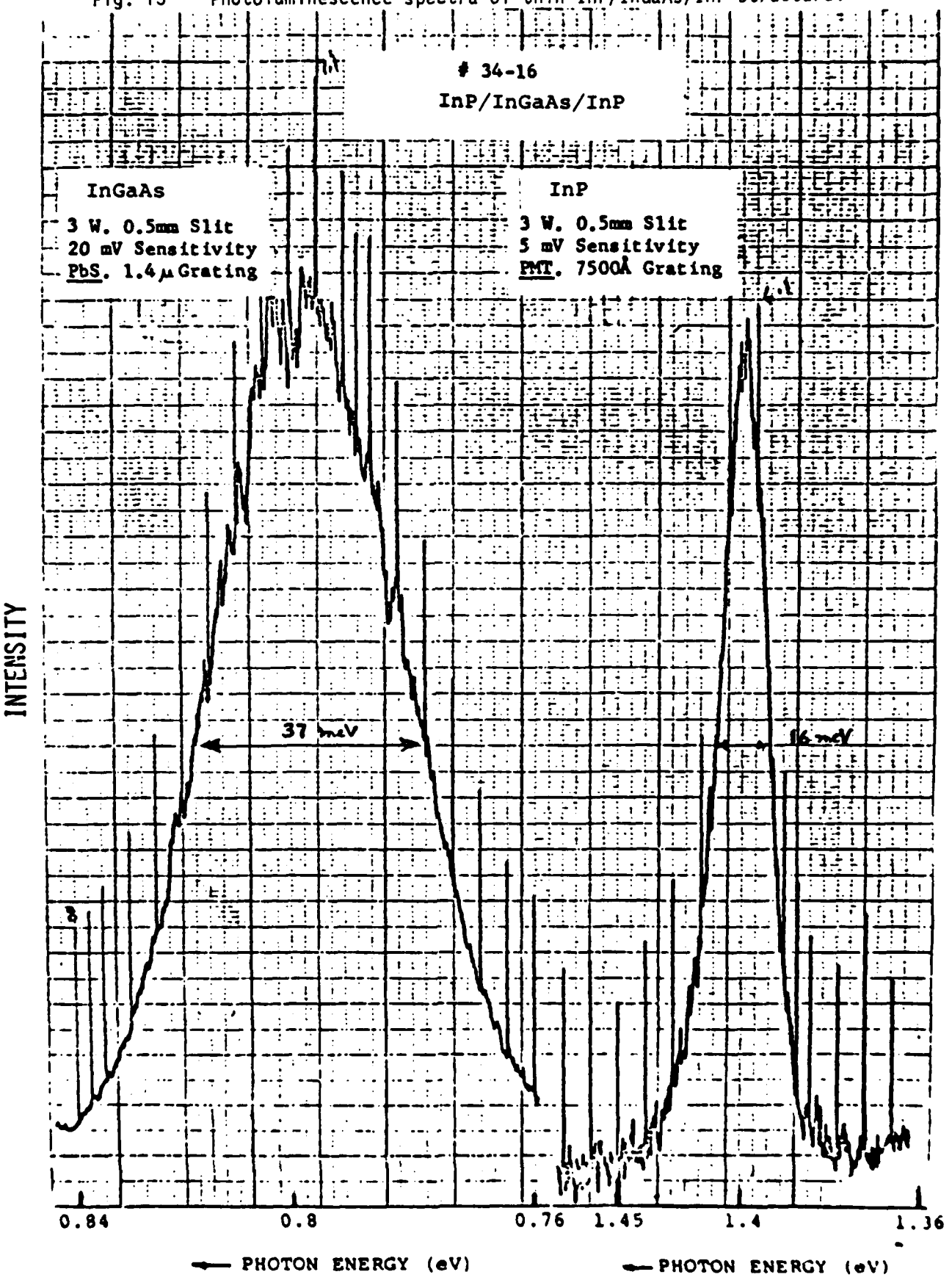
n-$In_{.53}Ga_{.47}As$ undoped

n-InP(s) substrate

5 μ

Fig. 12(b) A cleaved and stained section of InP/$In_{.53}Ga_{.47}As$ growth for photodiode fabrication.

Fig. 13 Photoluminescence spectra of thin InP/InGaAs/InP structure.



Mobilities measured in InGaAs material grown with different $\frac{III}{V} \frac{InCl + GaCl}{AsH_3}$ flow ratios is plotted in Fig. 14 and shows the peak mobility of 5826 $cm^2/V\text{-sec}$ at a 3:1 flow ratio and a background doping of $8 \times 10^{15} cm^{-3}$. The broken curve is for mobilities as a function of estimated III/V mole ratio and the peak mobility here appears to be at around 2:1 ratio. The use of HCl bottled in a steel cylinder possibly causes reduction in mobilities because of the reaction of HCl with the container, producing ferrous chloride. This, however, can be corrected by the use of Monel or stainless containers. Out diffusion of Fe from the InP substrates could also contribute to low mobilities.

The recommendations for future work to improve the mobility of VPE InGaAs are:

(1) Replacement of the stainless-steel gas lines with Monel lines,

(2) Using $AsCl_3$, which has been tried a little without any attempt to ensure lattice matching (was never checked using a single-crystal diffractometer),

(3) Using better quality arsine (better than 5-9's).

The lattice mismatch is around 0.02%[13] and hence is not the cause of the low mobility.[24]

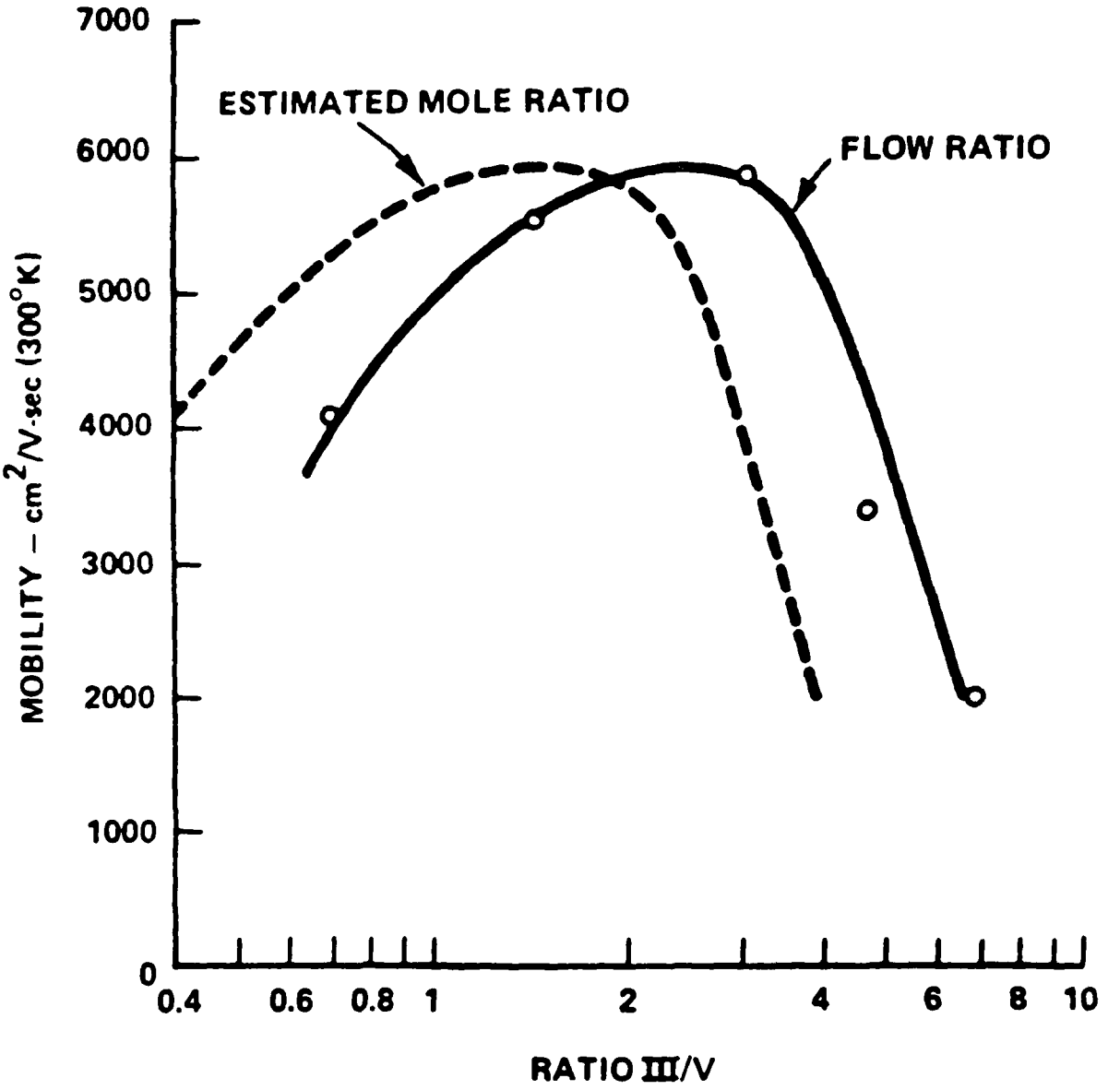


Fig. 14 Electron mobility of $In_{.53}Ga_{.47}As$ as a function of III/V ratio in gas phase.

3. DEVICE EVALUATION OF 33% InGaAs ON GaAs

As reported in Interim Technical Report No. 1 of this contract, near to the end of that reporting period, a new reactor was built which incorporated the facility for H_2 bypass flow. Little or no bluish haze was observed for wafers grown with the H_2 bypass flow, and the quality of the growth appeared to have improved also as indicated by narrower photoluminescence peaks. Wafer InG 45-2 (29% In, 7.1 micron buffer layer grown on a Cr-doped (100) GaAs substrate of which 0.65 micron was constant composition, with no active layer) and wafer InG 46-1 (33% In, 10.7 micron buffer layer of which 1.1 microns was constant composition, with an active layer included) were two of the best wafers grown in this new reactor using H_2 bypass flow. Both surfaces had a faint amount of cross-hatch, with wafer InG 45-2 having a photoluminescence half-width of only 20 meV, while wafer InG 46-1 had a half-width of 50 meV. Of all the techniques tried during that reporting period in order to improve the surface quality, it appeared that the H_2 bypass was the only one to significantly reduce the growth dislocations to acceptable levels.

During the first part of this reporting period, FETs were fabricated on wafer InG 46-1 for purposes of evaluation. The FET device geometry used is shown in Fig. 15. The gate width Z is 150 microns and the length L is in the 0.3-0.4-micron range. The Au gates were defined by electron beam exposure of PMMA resist, and Au-Ge/Ni/Au was used for the ohmic contacts. The fabrication sequence in order was: mesa etch, ohmic contact formation, gate deposition, and Au overlay.

Figures 16-19 give the drain characteristics of devices 46-0, 46-1, 46-4 and 46-5 after they were bonded into an amplifier circuit. Presumably, the higher g_m of 46-0 (20 mmhos vs. 14 mmhos) is due to variations in the doping across the wafer, since this variation was seen in probing devices across the wafer. There seemed to be some deteriora-

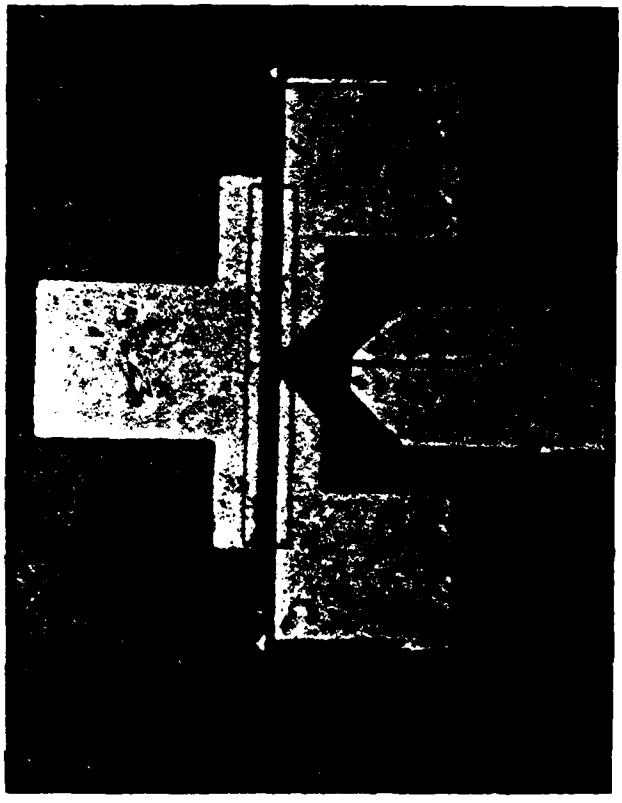


Fig. 15 Device geometry used for InGaAs FETs.

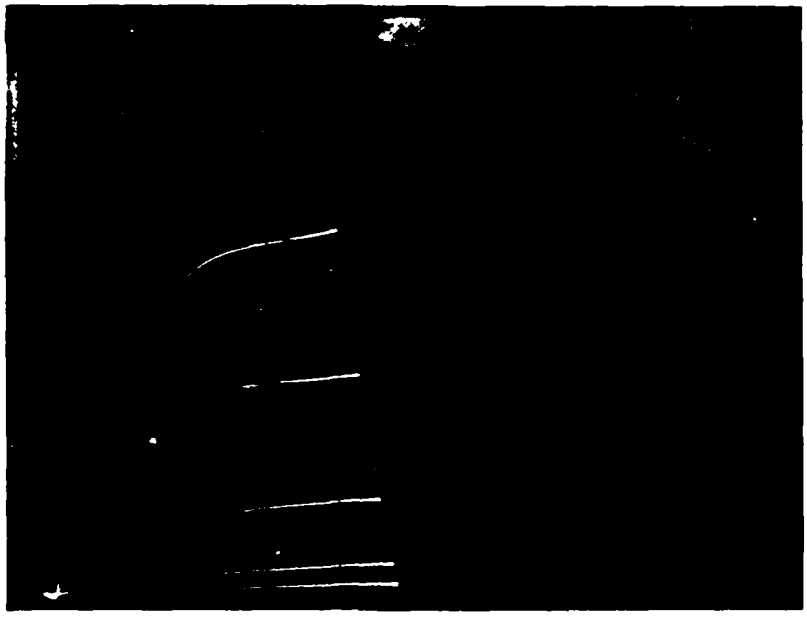


Fig. 16 Drain characteristic of 46-0.
(5 mA/div, 0.5V/div, 0.5V/step)

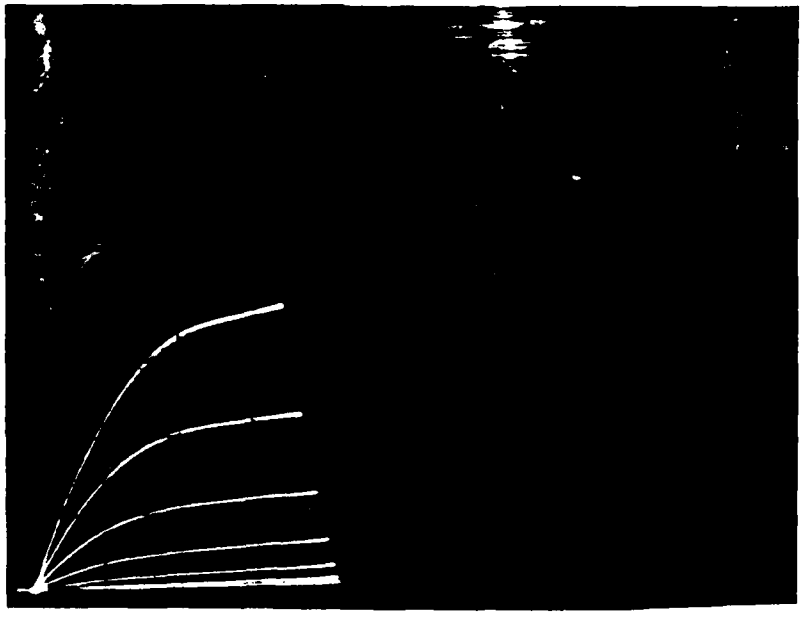


Fig. 17 Drain characteristic of 46-1.
(5 mA/div, 0.5V/div, -0.5V/step)

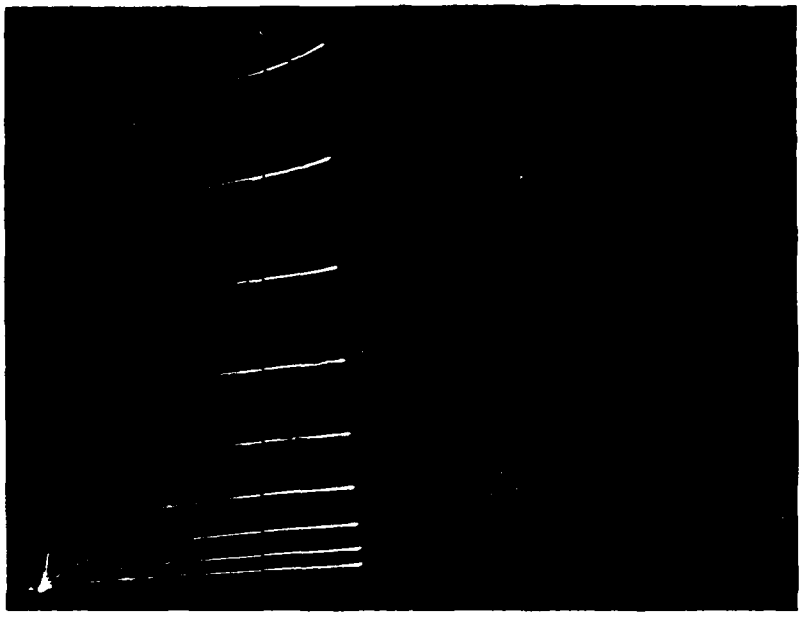


Fig. 18 Drain characteristic of 46-4
(2 mA/div, 0.5V/div, -0.2V/step).

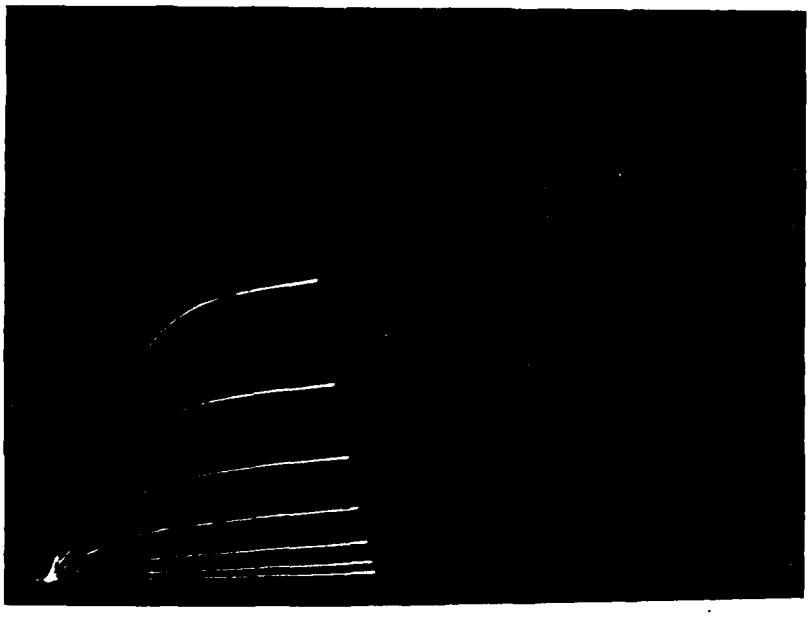


Fig. 19 Drain characteristic of 46-5
(5 mA/div, 0.5V/div, -0.5V/step).

tion in the gate leakage during bonding of the devices. Device 46-0 shorted when the drain bias was taken above 3.5 V, as did several other devices that were bonded up.

Table II summarizes the 8-GHz rf performance for Wafer 46-1.

TABLE II

8-GHz Performance for Wafer InG 46-1

Device	MAG (dB)	NF_m (dB)	G_a (dB)	V_g, V_d at NF_m (V)
46-1	17.3	3.15	14.2	-0.44, 2.57
46-4	14.5	3.62	12.3	-0.261, 3.44

Devices 46-4 and 46-5 were bonded up into s-parameter fixtures and the y-parameter data shown in Appendix A were obtained. The input resistance, r_{in}, was computed from this data using Eq. (1):

$$r_{in} = \frac{g_{11}}{g_{11}^2 + (b_{11} + b_{12})^2} \tag{1}$$

and the results are shown in Table III.

TABLE III

Device Parameters for Wafer InG 46-1

Device	r_{in} (ohms)	R_s (ohms)	dc g_m (mmhos)	2-GHz g_m (mmhos)
46-4	17.5	15	14.5	10.9
46-5	27.8	14	14.0	10.9

The reduction in g_m with frequency is believed to be due to traps. It is also seen for GaAs FETs made on MBE material.

Appendix A of Interim Technical Report No. 1 of this contract outlined the technique of determining the effective saturated drift velocity, v_s, from the drain characteristics of FET devices. Using a barrier height of 0.41 eV[16], the plots shown in Fig. 20 were obtained. With the exception of device 46-0, all the plots have quite large "tails" which previously were attributed to velocity degradation at the active-layer buffer-layer interface.[7] Only small tails were seen for the wafers of the previous reporting period[17] (wafers InG 37-9, InG 37-11 and InG 40-4). These latter wafers were all moved ~8 cm from the buffer layer growth position to the active layer growth position (ΔT = 18°C). The sequencing was the shut-off of the Cr, the moving of the wafer, and the turning-on of the H_2S (all in ~1/2 min. compared to an active layer growth time of 15 min.). The wafers were originally upstream from the H_2S line, but downstream from the Cr line. Wafer InG 46-1, on the other hand, was downstream from both lines and hence was not moved between the buffer- and active-layer growths. The Cr was shut off, the H_2 bypass was shut off, and then the H_2S solenoid was turned on. Thus, there is no reason why any kind of material quality change should occur at the buffer-active layer interface for wafer InG 46-1.

The tails in Fig. 20 could be attributed to a gradual rise in the doping profile. If so, there still would be the question as to why device 46-0 appears to have a sharper doping profile. Due to leakage current, doping profiles could not be obtained by the doping profiler. An effort was made to obtain a C-V plot and convert this to a doping profile by software. The capacitance meters are relatively insensitive to leakage current because of their higher frequency operation (1 MHz), but pay for this by being very sensitive to series resistance. Fig. 21 shows the C-V plot for a 9-mil dot on wafer InG 46-1, showing the effect of series resistance by the peak in the capacitance. If C_t is the true capacitance and r the series resistance, then assuming the measured capacitance C_m is given by:

$$C_m = \frac{C_t}{1 + \omega^2 r^2 C_t^2} \quad ,$$

then at the peak $C_t = 2\ C_m$ and $\omega r = 1/C_t$, assuming r is constant. C_t can now be computed for each value of C_m, and this plot is also shown in Fig. 22. Figure 23 shows the doping profile obtained from this corrected C-V curve. This plot indeed shows a gradual slope to the doping profile which would account for the tails in Fig. 20. An increase in r near pinchoff due to the increased resistance from the interior of the dot to its outer edge might be responsible for the slope in the doping profile. The only way to be certain is to obtain a C-V profile at 100 KHz to eliminate the effects of series resistance with a technique or an instrument which is not sensitive to shunt conductance. Even so, one still has to worry about the leakage current self-biasing the interior part of the dot so that pinchoff is extended to higher voltages, again effecting a slope in the doping profile.

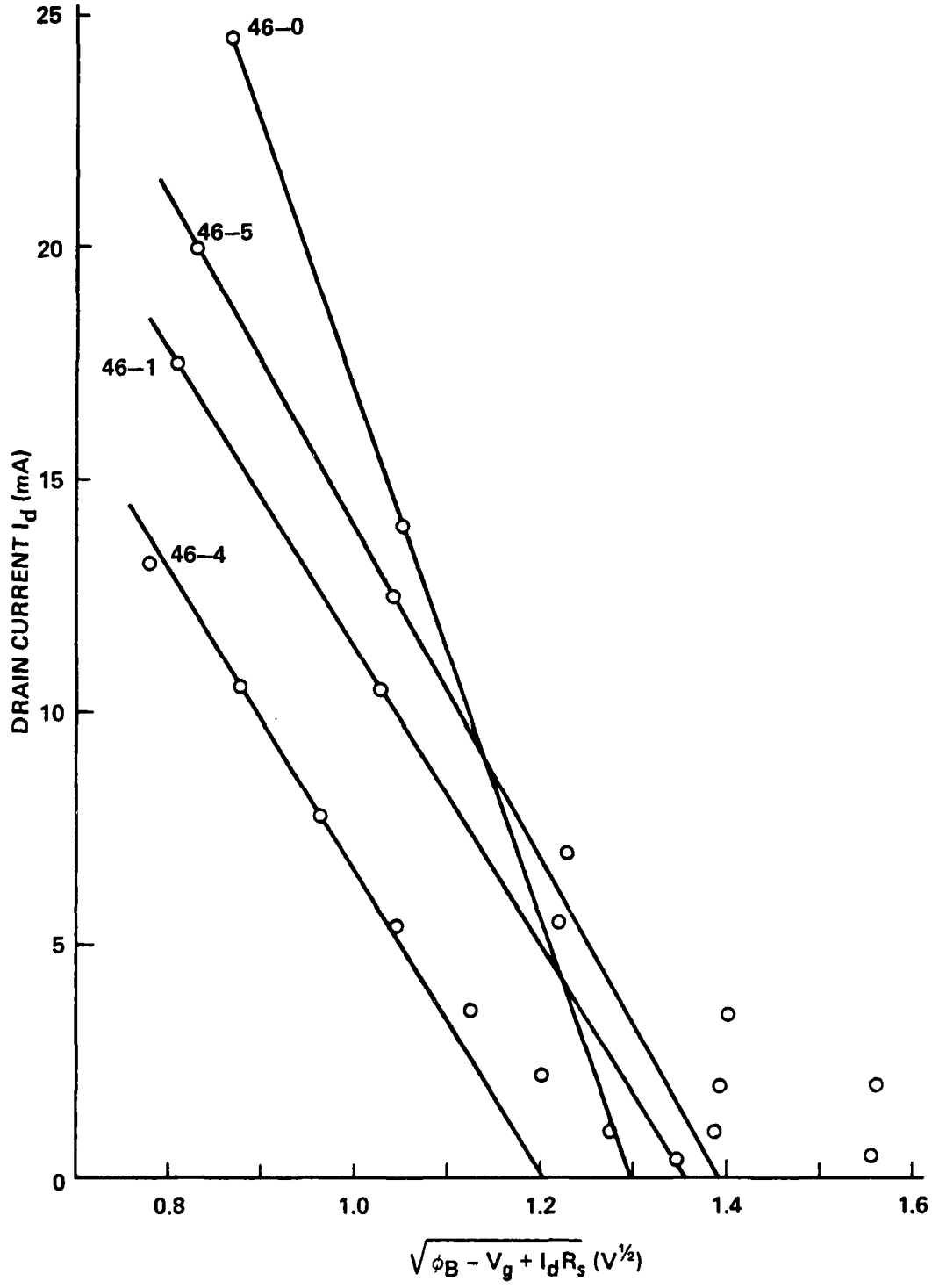


Fig. 20 Effective saturation velocity determination for run 46-1.

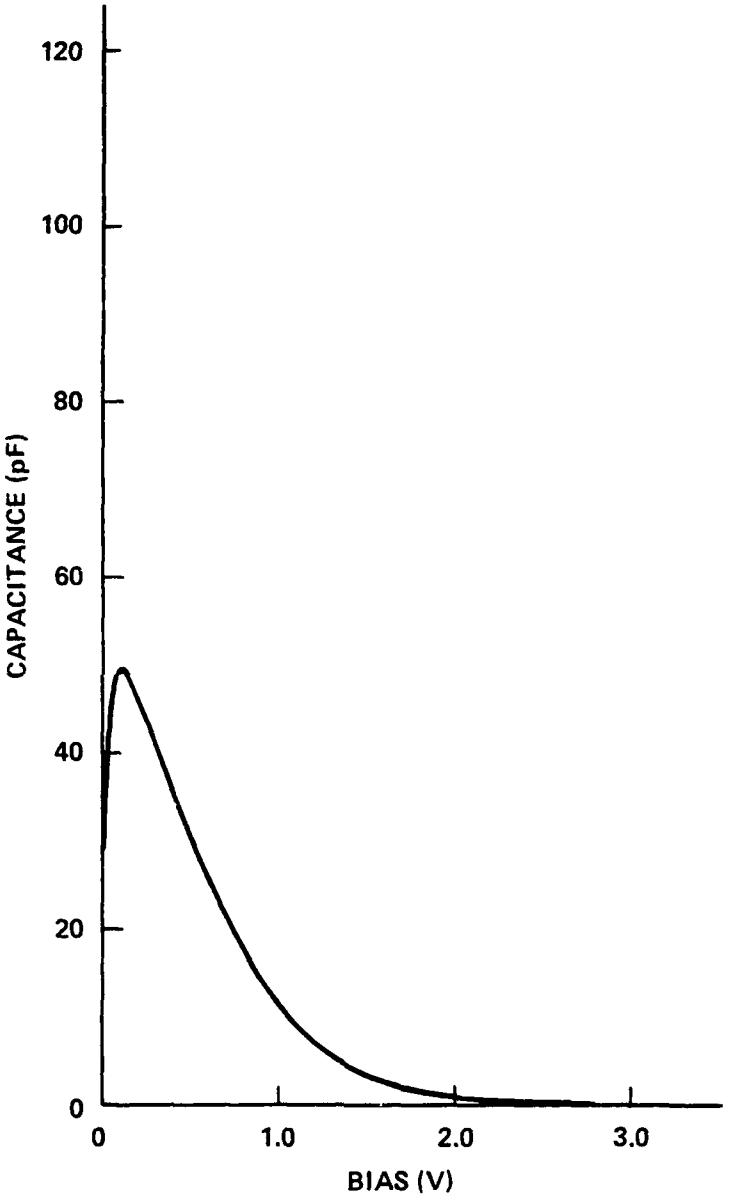


Fig. 21 C-V profile of wafer 46-1.

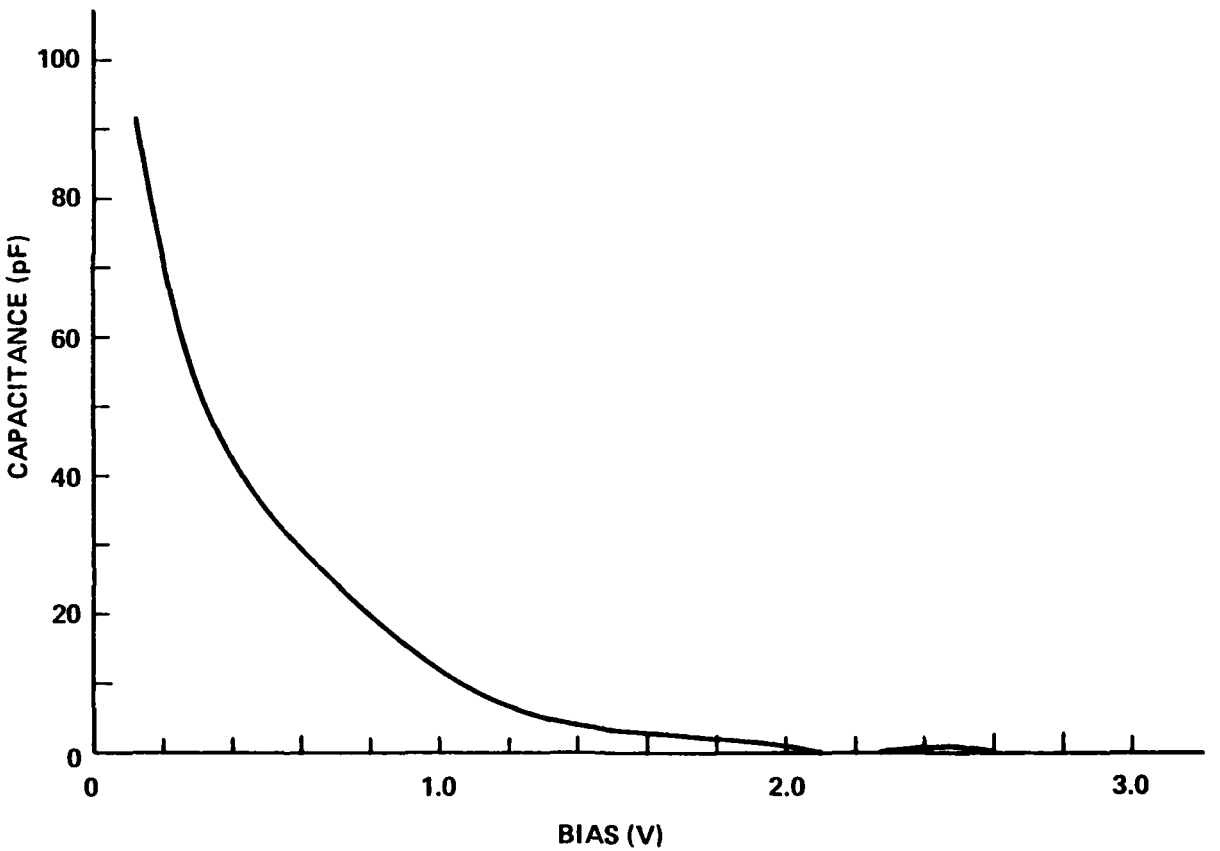


Fig. 22 C-V plot corrected for series resistance.

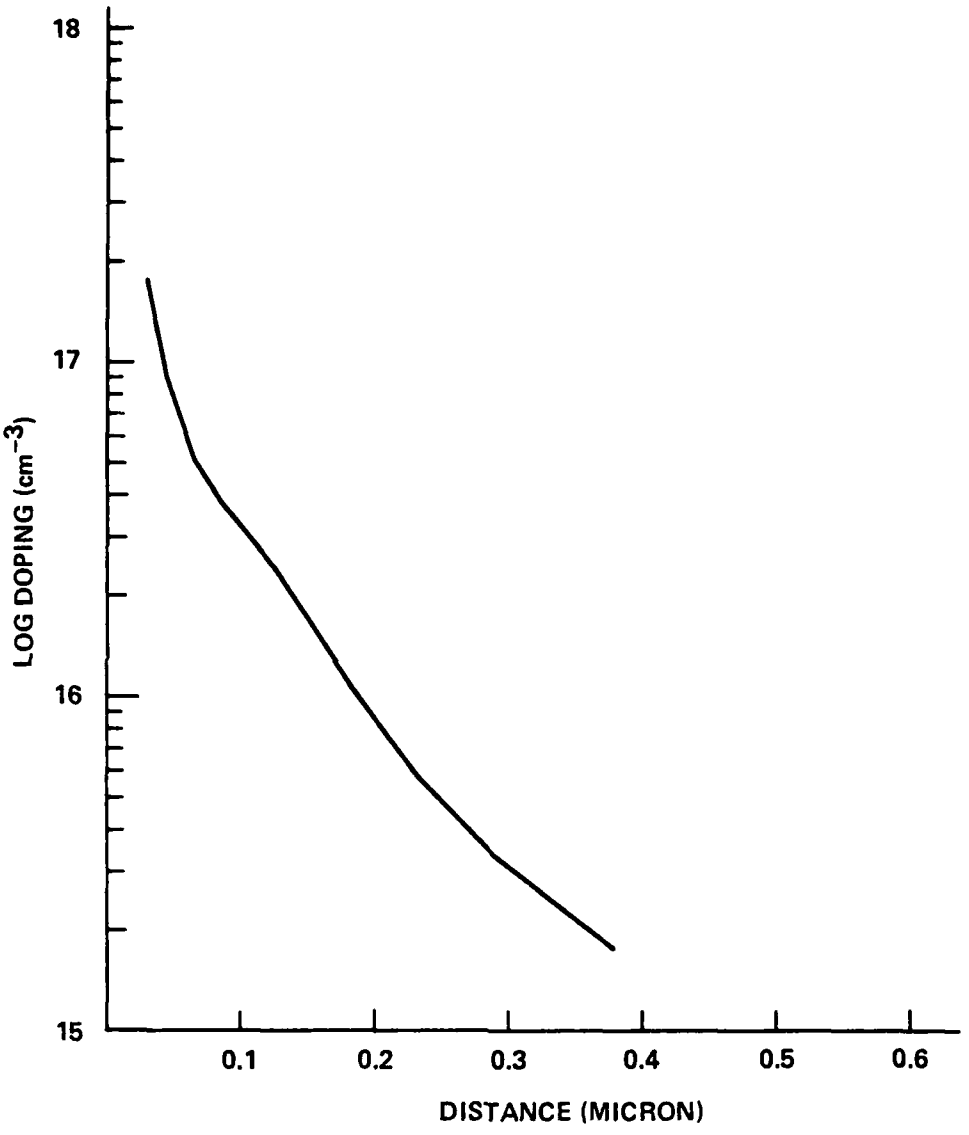


Fig. 23 Doping profile obtained from data of Fig. 22.

It is necessary to know the doping profile in order to compute v_s from the curves of Fig. 20. To obtain a value of 1.79×10^7cm/sec as was obtained for run #55 (34% In),[7] a doping of $5.8 \times 10^{16}cm^{-3}$ would be needed for devices 46-1, 46-4, and 46-5, while 46-0 would need $1.5 \times 10^{17}cm^{-3}$. If the doping is higher than these values, the computed value of v_s will be lower. Although it is possible for the doping level to vary across the wafer (to account for the difference between device 46-0 and the rest of the devices), it doesn't seem possible that there could be the difference in the rate of buildup of the doping across the wafer needed to explain the tail differences in Fig. 20.

The values of NF_m in Table II are rather high. Using Fukui's equation for NF_m,[18]

$$NF_m = 1 + kf\, L^{5/6} \left(\frac{N_d}{a}\right)^{1/6} Z^{1/2}\, (r_g + R_s)^{1/2} \qquad (2)$$

and using upper limit values for the parameters ($L = 0.4$ μm, $r_g + R_s = 27.8$ ohms without subtracting out $g_m L_s/C_{gs}$) and assuming $N_D = 10^{17}cm^{-3}$ (NF_m only weakly dependent upon N_D), then $NF_m = 2$ dB using $k = 0.04$ for GaAs.[19] The computed value is way below the measured values of 3-3.5 dB, in spite of using upper limit values and the value of k for GaAs (k is a materials parameter, and the whole reason for going to InGaAs is the hope that it will be significantly lower than it is for GaAs). With the bias conditions for NF_m given in Table II, the gate leakage was measured to be 0.9 μA. The shot noise associated with this current gives an insignificant contribution to the noise figure, whether placed across the gate capacitance or as feedback from drain to gate. It does not appear, then, that gate leakage is responsible for the high value of NF_m.

Summarizing, uncertainty in the doping profile prevents determination of the effective saturated velocity v_s. The uncertainty in the doping, however, does not prevent the determination that the measured values of minimum noise figure NF_m are considerably higher than the computed values for GaAs having the same parameters. If v_s is below the 1.3×10^7 cm/sec value typically found for GaAs, the higher values of NF_m could be expected. The surface appears as good, if not slightly better, than the surface of Run #55 (34% In) for which v_s was determined to be 1.79×10^7 cm/sec. It appears that the wide photoluminescence half-width is a better indicator of material quality than the optical appearance of the surface.

4. FABRICATION AND EVALUATION OF FET DEVICES ON 53% InGaAs

4.1 FET Fabrication

The same device geometry and fabrication sequence was used as described in Section 3 and shown in Fig. 15. With the epitaxial structure shown in Fig. 4 to minimize gate leakage, the only change needed in the fabrication process was the mesa etch.

Because of the two-layer structure, two etching steps were needed for the mesa etch. HCl was used to etch the top InGaAsP (or InP) layer and 3:1:1 H_2O:HF:H_2O_2 etch was used for the InGaAs layer. When positive resist was used as the mesa mask, the HCl etch undercut the resist to the extent of almost eliminating the InGaAsP layer. This problem was solved by going to CVD SiO_2 as the mesa mask. However, with the InGaAsP layer acting as the mask for the InGaAs layer; the InGaAs would etch preferentially, producing a positive slope in one direction and a negative slope in the other direction (Fig. 24). This overhang would cause a discontinuity in the ohmic contact and gate metallizations. To solve this problem, the mesa patterns were redefined with positive photoresist after the InGaAsP etch. Because of the slight amount of undercutting of the SiO_2 during the InGaAsP etch, the photoresist extended out over the InGaAsP edge to prevent the InGaAsP from acting as a mask. The slight undercutting of the photoresist during the InGaAs etch eliminated the negative-sloped overhang and resulted in the mesa edge profile shown in Fig. 25. An advantage of such a two-step profile is that the InGaAs (or InP) and InGaAs thicknesses can be determined for each device by Nomarski interferometry (because of thickness variations across the wafer, this ability can be very important). The disadvantage of the profile is that the gate metal contacts the InGaAs layer at three points where it crosses the mesa edge, thus increasing the gate leakage.

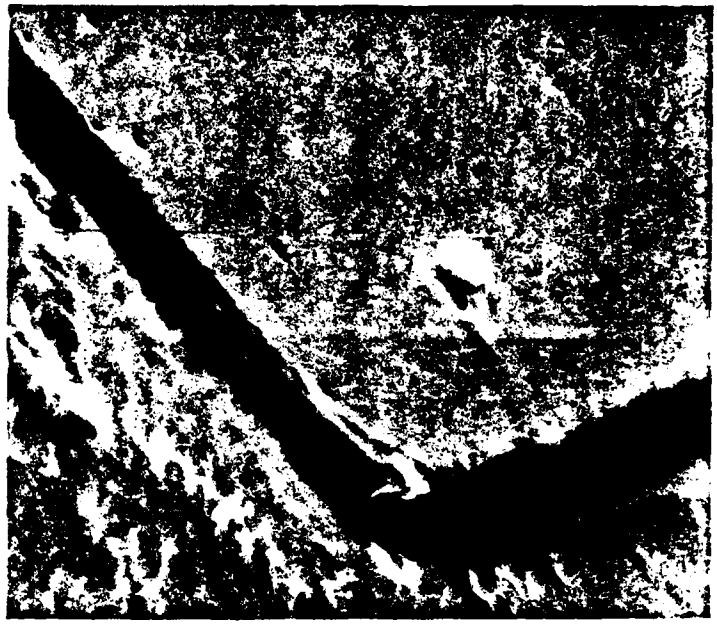


Fig. 24 Mesa edge profile for InGaAsP on InGaAs.

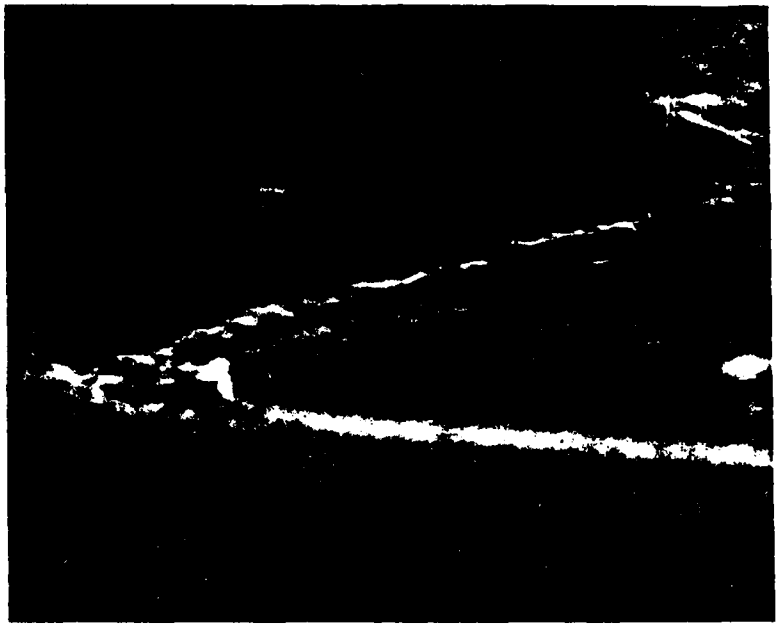


Fig. 25 Improved mesa edge profile.

4.2 LPE Material (1.27-eV InGaAs/InGaAs)

4.2.1 General Comments

The initial wafers processed were either ruined by faulty mesa etches as discussed in Section 4.1, or had such thick layers that current saturation could not be achieved without shorting the drain to the source. Some of the wafers showed little or no rectification when Au dots were evaporated on them for purposes of doping determination, signifying either a discontinuous or a very thin InGaAsP layer.

Due to leakage current, none of the wafers could be profiled for doping by the 100-kHz doping profilers. Some of the wafers were profiled by obtaining 1-MHz C-V data and converting this to a doping profile by software. As mentioned in Section 3, this technique is plagued by series resistance inaccuracies and a considerable amount of time can be spent in trying to correct for this effect. Consequently, not all the wafers processed for devices had reliable doping profiles. The wafers were too small to afford cleaving off a section for purposes of future doping evaluation in case the device run was successful.

4.2.2 Device Run L6-4

Device run L6-4 made on wafer L6-4 was the first run from which working devices were obtained. No doping profile was made on this wafer; however, van der Pauw measurements made on previous growths from the same melts indicate a doping of $1.75 \times 10^{16} cm^{-3}$ for the InGaAsP layer and $1.66 \times 10^{17} cm^{-3}$ for the InGaAs layer. Using Nomarski interferometry on the mesa edges of several of the devices, the InGaAsP layer was found to be about 800-850 Å thick and the InGaAs layer was 4100-4200 Å thick. The device gate lengths were around 0.4 micron.

Figure 26 shows the drain characteristics of two of the devices and Fig. 27 shows the reverse leakage characteristic of a device. The InGaAs layer is far too thick to be pinched off, with gate leakage preventing much more than -4 V being applied to the gate. This, of course, will prevent NF_m from being measured. In trying to minimize the noise anyway, a range between 15 and 18 dB was measured at 8 GHz with only at most a couple dB of associated gain. Device L6-4-2 gave NF_m = 18 dB with G_a = 2 dB. The devices tended to oscillate easily.

S-parameter measurements were made on devices L6-4-1, 2, and 3, and the results are shown in Appendix A. Table IV gives the 8-GHz parameters g_{11}, g_{21} and g_{22} for these devices, along with the same parameters for GaAs devices from run EB 26 fabricated under Contract N00014-77-C-0655. Run EB 26 had values of NF_m ranging from 1.2-1.5 dB and associated gains of 13-14 dB.

TABLE IV

8-GHz y-Parameters for Run L6-4

Device	L6-4-1	L6-4-2	L6-4-3	EB 26-1	EB 26-2	EB 26-4	EB 26-5
g_{11} (mmho)	1.46	5.76	1.85	1.78	1.04	.986	1.02
g_{21} (mmho)	5.95	11.1	6.61	19.7	17.2	17.6	20.1
g_{22} (mmho)	22.0	8.78	18.9	4.54	4.79	4.28	4.41
MAG (dB)	-5.6	-2.15	-5.05	10.8	11.7	12.6	13.5

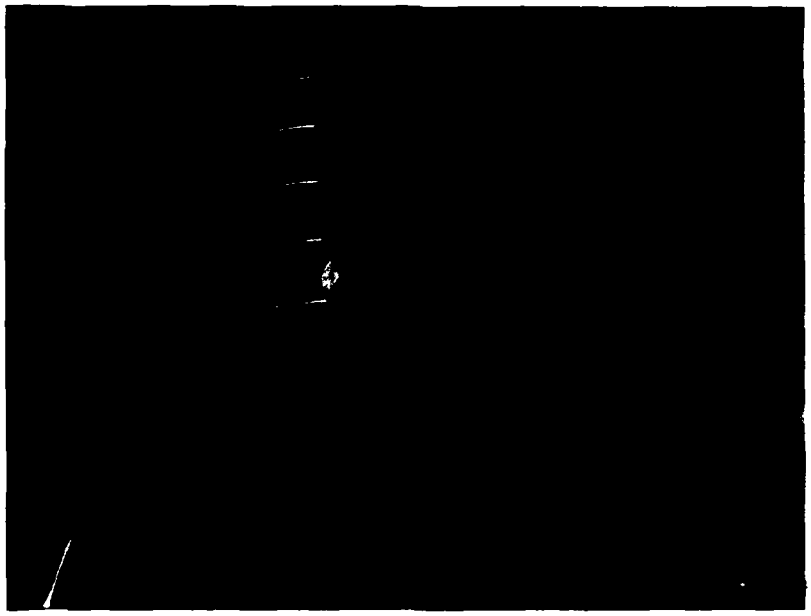


Fig. 26(a) Device L6-4-1.

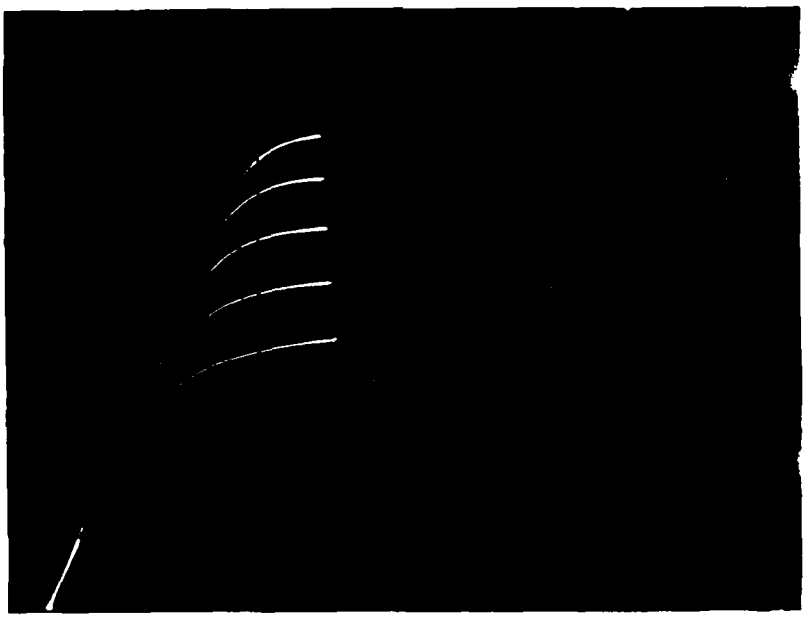


Fig. 26(b) Device L6-4-3.

Fig. 26 Drain characteristics for run L6-4.
(20 mA/div, 1V/div, -1V/step).

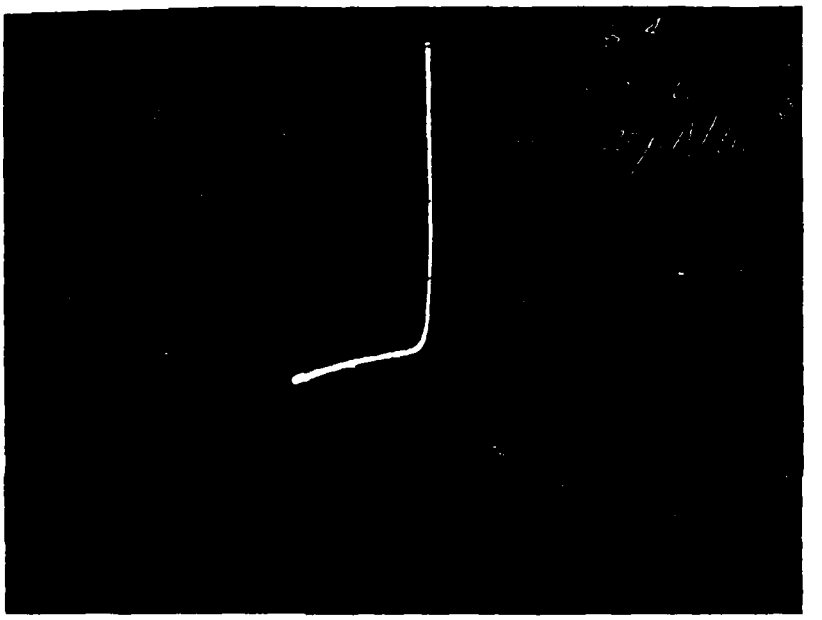


Fig. 27 Device gate characteristic for run L6-4.

Ignoring feedback and assuming $|y_{21}| \cong g_{21}$, then the maximum available gain is given by[20]

$$MAG = \frac{g_{21}^2}{4\, g_{11}\, g_{22}} \qquad (3)$$

which is also shown in Table IV. With the exception of L6-4-2, the input conductance of run L6-4 is comparable to that of run EB 26. The values of g_{21} are somewhat lower than those for run EB 26, but this is due to the lower doping ($1.7 \times 10^{17} cm^{-3}$ vs. $3.5 \times 10^{17} cm^{-3}$) of the channel and the lack of an n^+ layer to lower the source resistance, and also to the slight amount of g_m compression near zero gate bias. This g_m compression might be due to the lower v_s InGaAsP layer[21] and perhaps penetration of the phosphorus from the InGaAsP into the InGaAs layer during growth (indeed, the PL peak of the InGaAs shifts after the InGaAsP growth).

Table IV reveals a considerable output conductance for run L6-4. Presumably, this could be due to the thickness of the channel where the channel is actually thicker than the gate length. The output shunt resistance varies as $\cosh(\pi L/2d)$[22] where d is the channel thickness, indicating the exponential dependence that this shunt conductance has on the L/d ratio.

4.2.3 Saturated Velocity Determination

In spite of the devices of run L6-4 having poor noise and gain performance because of a very thick channel, the device drain characteristics can be used to determine the effective saturated velocity v_s.

For the doping profile shown in Fig. 28, where w is the gate depletion edge, then

$$w = \sqrt{(\phi_B - V_g)\,\frac{2\varepsilon}{qf\,N_D}} \qquad 0 < w < d_1 \qquad (4)$$

$$= \sqrt{(\phi_B - V_g)\,\frac{2\varepsilon}{qN_D} + (1-f)\,d_1^{\,2}} \qquad d_1 < w < d_2 \qquad (5)$$

where ϕ_B is the barrier height of the gate and V_g is the gate bias. Assuming the channel completely velocity saturated at a value of v_s, then for $0 < w < d_1$,

$$I_d = qZN_D \int_{d_1}^{d_2} v_s dx + qZfN_D \int_{w}^{d_1} v_s dx \qquad (6)$$

and by Eq. 4,

$$\frac{\partial I_d}{\partial \sqrt{\phi_B - V_g}} = - v_s Z \sqrt{2\varepsilon q f N_D} \quad . \qquad (7)$$

If $d_1 < w < d_2$, then

$$I_d = qZN_D \int_{w}^{d_2} v_s dx \qquad (8)$$

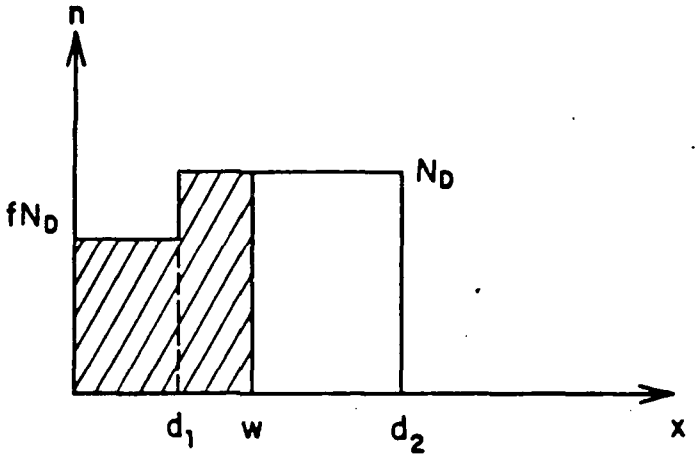


Fig. 28 Channel doping profile and gate depletion region edge.

and by Eq. 5 ,

$$\frac{\partial I_D}{\partial \sqrt{(\phi_B - V_g) + (1-f)\, d_1^2 \left(\frac{qN_D}{2\varepsilon}\right)}} = - v_s Z \sqrt{2\varepsilon q N_D} \qquad (9)$$

so that a plot of I_d vs w where w is given by Eq. 5 will yield a slope from which a profile of v_s across the InGaAs can be determined.

For Run L6-4, d_1 = 850 Å, $fN_D = 1.75 \times 10^{16} cm^{-3}$ and $N_D = 1.66 \times 10^{17} cm^{-3}$, so the voltage to deplete the InGaAsP should only be 0.1 V. Thus, a barrier height of ϕ_B = 0.5 eV[21] should deplete the InGaAsP and Eq. 5 is the appropriate equation. Including the voltage drop $I_d R_s$ across the source resistance as part of V_g and using R_s = 8.2 ohms yields the plot shown in Fig. 29 using the drain characteristic of device L6-4-1 shown in Fig. 26(a). With Z = 151 microns, the steepest portion of the plot yields by Eq. 9 an effective saturated velocity of

$$v_s = 2.95 \times 10^7 \text{ cm/sec}$$

which is considerably higher than the value of 1.3×10^7 cm/sec obtained using the same technique on GaAs FETs. This represents over a factor of two improvement in v_s over GaAs, and substantiates the reasoning given in the Introduction as to why InGaAs should be given serious consideration as a viable FET material. Figure 29 indicates that the velocity v_s gradually deteriorates as the InGaAsP-InGaAs interface is approached, and, as has already been suggested, this may indicate some penetration of the phosphorus into the InGaAs during growth. The fact that the gate length is longer than the channel thickness may cause a g_m reduction so that v_s may actually be higher.

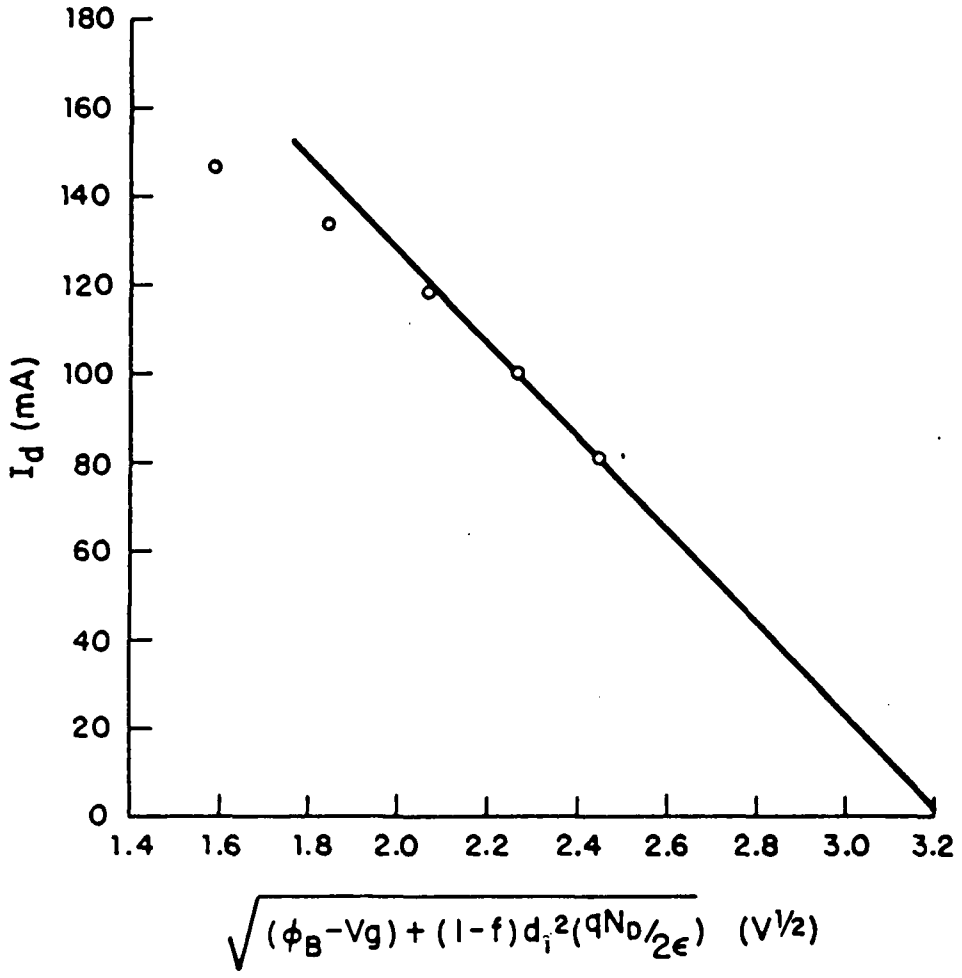


Fig. 29 Effective saturation velocity determination for run L6-4.

4.2.4 Efforts to Achieve Thinner InGaAs

For all of the LPE wafers grown which had their layer thicknesses measured by Nomarski interferometry, the InGaAsP layer was around 1000 Å or less, while the InGaAs layer was considerably thicker, around 3000-4000 Å. Both growths take about 1 sec each, indicating that the InGaAs grows considerably faster than the InGaAsP (unless the phosphorus depletes out of the InGaAsP into the InGaAs to render a large portion of the InGaAsP insoluble in HCl so that it is considered part of the InGaAs). Since it is hard to control LPE growths of less than 1 sec (about the time it takes to push the boat in and then out from under the melt), the plan was to grow the InGaAs and then thin it to around 1500 Å and grow a 1000-Å-thick InP layer over it by VPE.

The technique used was to coat the whole wafer with black wax except for the outside border. The InGaAs was then removed from the borders with 3:1:1 H_2O:HF:H_2O_2, the black wax was removed, and the step height was measured. The wafer was then thinned with 4:$\frac{1}{40}$:1 H_2SO_4:H_2O_2:H_2O (which is a slower etch than the 3:1:1 etch) until the desired step height was reached.

After perfecting the technique on several dummy wafers, wafer LP4/16-5 was thinned from ~2000 Å to ~1500 Å. The VPE InP layer grown above this layer was filled with scratches, presumably from damage to the InGaAs incurred when the black wax was cleaned off with a Q-tip. The wafer was unusable, but presumably the technique might be made to work with a little more effort. However, since it appears that InGaAs layers as thin as 2000 Å can be grown by LPE (the layers used for the thinning study were grown by a different operator than were the InGaAsP on InGaAs layers), an effort was made to retry growing InGaAsP on InGaAs by LPE again.

Wafer LP4/29-2 was grown having 1130 Å of InGaAsP and 340 Å of InGaAs, being too thin to use. Wafer LP4/29-1 had 1250 Å of InGaAsP and 3100 Å of InGaAs, and although this InGaAs thickness is double the desired value, it is at least 1000 Å thinner than it was for L6-4, so devices were fabricated on it. Figure 30 shows a typical device drain and gate characteristic, revealing the same problems that plagued run L6-4 -- a high pinchoff voltage and g_m compression. No further testing was done on the devices.

4.3 VPE Material (InP/InGaAs)

Although the mobility of the VPE InGaAs is considerably lower than for the LPE InGaAs (5500 cm^2/V-sec for $10^{17} cm^{-3}$ doping), it is still higher than for GaAs and enables thinner layers to be grown than by LPE.

Figure 31 shows the drain and gate characteristics of a device fabricated on VPE wafer Q35-8 (run Q35-8). This wafer had an InGaAs thickness of 1430 Å and an InP thickness of 920 Å with a doping of around $10^{17} cm^{-3}$ for both layers. Maximum g_m occurs at about V_g = -4 V and is 25 mmhos, which is higher at -4 V than was LPE device L6-4-1 for a lower doping, so it appears that a high value of v_s exists for the VPE material also.

Table V gives the 8-GHz rf data for three devices from this run.

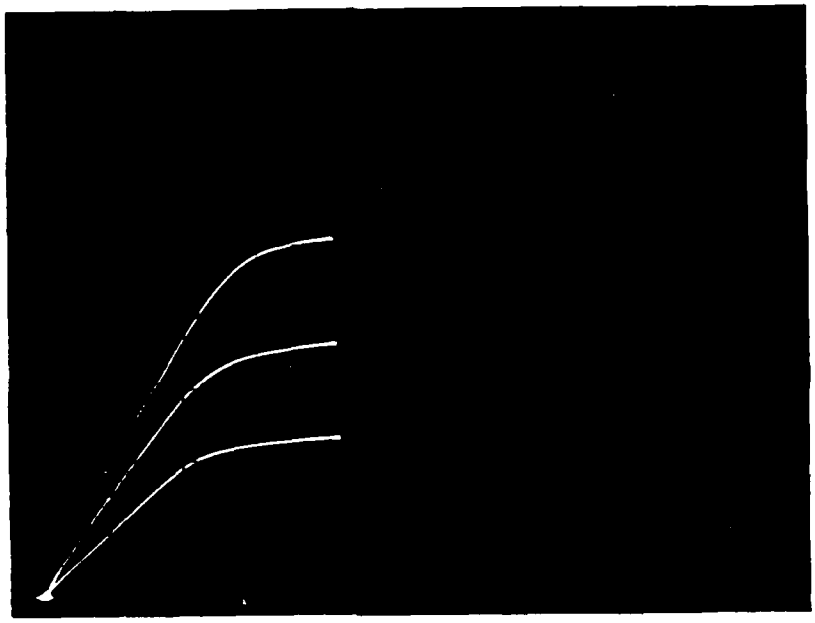
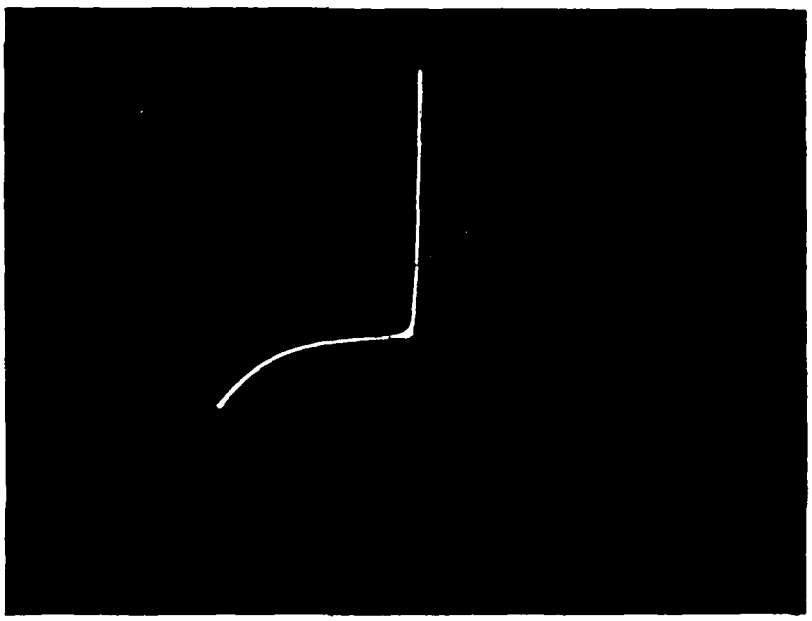


Fig. 30(a) Drain characteristic
(20 mA/div, 1V/div, -2V/step).



(b) Gate characteristic
(1 mA/div, 1V/div).

Fig. 30 Device characteristics for Run 29-1.

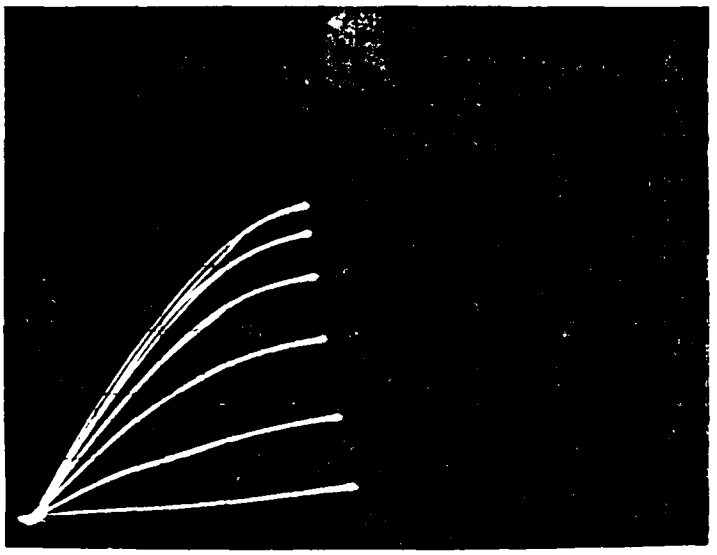


Fig. 31 Drain characteristic for run Q35-8.
(20 mA/div, .5V/div, -1V/step)

TABLE V

8-GHz Performance for Wafer Q35-8

Device	MAG (dB)	NF_m (dB)	G_a (dB)	V_g at NF_m (dB)
35-8-1	10	11.1	5.6	- 1.79
35-8-2	12	10.3	6.8	- 2.96
35-8-3	12	9.5	7.0	- 2.33

The values of NF_m are very high. In hopes of understanding what the problem might be, s-parameter measurements were made on devices Q35-8-2 and 3 and the data is shown in Appendix A. A -3 V gate bias was used for this data to achieve maximum g_m and to obtain the parameters at the bias at which NF_m was measured.

Table VI gives the 8-GHz y-parameters for these devices from run EB 26 fabricated under Contract N00014-77-C-0655. Run EB 26 had values of NF_m ranging from 1.2-1.5 dB and associated gains G_a of 13-14 dB. The y-parameters for both runs agree remarkably well with the exception of the feedback parameter y_{12} which is much lower for Run Q35-8. The lower value of y_{12} is because of being near a zero-crossing and probably not because the feedback parameters are any less (the data for run EB 26 was taken near zero gate bias in contrast with the -3V bias used for run Q35-8). With gate lengths of around 0.4 micron, Table VI indicates that according to Eq. 2, NF_m is not higher for Run Q35-8 because of its small-signal circuit model parameters. This suggests that its noise sources are larger, which would be included in the parameter k in Eq. 2. More investigation of this needs to be done, especially to see if gate leakage current is responsible for the noise.

TABLE VI

8-GHz y-Parameters for Run Q35-8 (mmho)

Device	Q35-8-2	Q35-8-3	EB 26-1	EB 26-2	EB-26-4	EB 26-5
g_{11}	1.4	2.46	1.78	.946	1.06	1.02
b_{11}	8.85	7.58	12.7	10.8	10.1	11.7
g_{21}	15.5	18.7	19.7	17.1	17.5	20.1
b_{21}	-4.16	-5.02	-7.19	-5.22	-5.03	-5.39
g_{12}	0.113	0.0590	0.163	0.335	0.251	0.191
b_{12}	-0.050	-0.0192	-0.272	-0.497	-0.234	-0.212
g_{22}	4.08	2.42	4.54	4.80	4.30	4.41
b_{22}	5.61	8.42	7.56	6.85	6.62	6.79

5. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

The main achievement during this reporting period was the measurement of a high saturated velocity of 3×10^7 cm/sec for $In_{.53}Ga_{.47}As$ when used as an FET material. Whereas previously the high mobility of $In_{.53}Ga_{.47}As$ was known, it has been confirmed in a quantitative manner that it also has a high saturated velocity when employed as an FET material, being over a factor of two higher than the 1.3×10^7 cm/sec value obtained for GaAs and thereby recommending $In_{.53}Ga_{.47}As$ as a potentially superior FET material.

FETs fabricated on LPE material had InGaAs layers that were too thick to pinch off so that the noise properties could not be measured. These thick layers also resulted in a high output conductance so that the power gain was very low. Also, there was some evidence of penetration of the phosphorus from the InGaAsP layer into the InGaAs layer.

FETs fabricated on lower-mobility VPE material also showed evidence of a high saturated velocity, but were unable to produce minimum noise figures lower than 9.5 dB at 8 GHz. These devices had the same y-parameters as GaAs devices having 1.2-1.5-dB minimum noise figures, suggesting that the InGaAs devices have higher noise sources, perhaps due to gate leakage.

Future work should involve improving the VPE InGaAs mobility as outlined in Section 2, and doing further analysis on the VPE FETs to determine the reason for the high noise figures. Also, the use of buffer layers should be incorporated. Alternative gate structures should also be investigated, such as an implanted p-n junction or doping the top InP cap p-type and then selectively etching it.

The impressive results of MBE InGaAs[23] indicate that this approach should be investigated. Cornell has achieved mobilities of 8800 cm^2/V-sec at 300°C for InGaAs lattice matched to InP at a doping of around $10^{16}cm^{-3}$. The best GaAs FET performance in our laboratories has been with MBE, which strongly indicates investigating the growth of InGaAs by MBE. This will circumvent the problem of achieving thin layers as encountered with LPE, and by avoiding the use of corrosive hydride and chloride gases as used with VPE, perhaps the problem of low mobilities can also be bypassed. Also, because of the lower growth temperature, perhaps the g_m compression seen for both the LPE and the VPE material, believed to be due to penetration of the phosphorus from the InGaAsP layer into the InGaAs layer, can be eliminated. While work on developing the MBE growth process progresses, interim work on improved VPE material to enable continuation of the device development program can be carried out.

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APPENDIX A

This appendix represents a compendium of y-parameter data for some of the devices.

PAGE 3: ANA#A5209/DEPT 0810 1/14/88
VARIAN METROLOGY LAB/C. NISHIMOTO
MBE FETS INGAAS

.00 VOLTS, .00 MA (MEAS 1) 46-4 VD=3.5V

FREQ (MHZ)	GA MAX DB	GU MAX DB	S21 DB	S12 DB	K MAG	U MAG
2000.000			.26	-40.57	.13	5.64
2500.000			.20	-39.46	.26	2.16
3000.000			-.01	-38.13	.46	1.04
3500.000		18.84	.26	-37.22	.54	.87
4000.000		16.57	.27	-36.55	.82	.54
4500.000			.67	-36.00	.47	1.02
5000.000			.79	-35.87	.44	1.11
5500.000		19.16	.77	-38.47	.70	.76
6000.000			.89	-38.36	.41	1.04
6500.000	19.33	17.06	.55	-42.04	1.10	.31
7000.000	20.43	16.09	.20	-42.26	1.02	.25
7500.000		15.19	.16	-38.24	.57	.32
8000.000		14.72	.18	-38.98	.96	.26
8500.000	14.60	13.50	-.83	-45.66	3.11	.10
9000.000	13.93	12.79	-.86	-41.44	2.28	.14
9500.000	14.47	12.13	-.89	-35.25	1.20	.24
10000.00		11.76	-1.51	-32.22	.74	.34
10500.00			-.89	-29.22	-.34	8.90
11000.00		11.17	-2.00	-28.13	.52	.50
11500.00		9.89	-2.69	-26.56	.63	.47
12000.00		10.64	-1.61	-23.26	.70	.72
12500.00			3.89	-15.73	-.19	6.25
13000.00			-1.03	-18.01	-.68	4.87
13500.00			-2.75	-15.99	-.54	3.40
14000.00		5.90	-3.45	-17.13	.02	.53

REF PLANE EXT(CM): IN= 2.70, OUT= 2.70

PAGE 2: ANA=A5209/DEPT 8810 :/14/80
VARIAN METROLOGY LAB/C. NISHIMOTO
MBE FETS INGAAS

.00 VOLTS, .00 MA (MEAS 1) 46-4 VD=3.5V

FREQ (MHZ)	Y11 MAG	Y11 ANG	Y21 MAG	Y21 ANG	Y12 MAG	Y12 ANG	Y22 MAG	Y22 ANG
2000.000	1.779	89	10.986	-6	.100	-88	1.926	53
2500.000	2.155	87	11.019	-7	.115	-87	2.213	57
3000.000	2.556	85	10.915	-8	.136	-86	2.566	59
3500.000	3.015	84	11.385	-10	.152	-85	2.933	62
4000.000	3.550	83	11.671	-11	.168	-85	3.443	63
4500.000	4.083	86	12.145	-11	.178	-84	3.842	69
5000.000	4.592	87	12.431	-12	.182	-83	4.321	71
5500.000	5.338	87	12.602	-13	.138	-89	4.959	73
6000.000	6.146	88	12.954	-14	.141	-79	5.666	76
6500.000	7.004	86	12.990	-15	.096	-63	6.467	76
7000.000	7.531	85	12.728	-16	.096	-28	6.913	76
7500.000	7.893	84	12.882	-17	.155	-20	7.089	76
8000.000	8.269	84	13.100	-17	.144	-33	7.428	77
8500.000	9.146	84	12.805	-17	.069	-0	8.182	78
9000.000	9.688	83	12.324	-19	.115	61	8.757	78
9500.000	10.297	83	12.664	-20	.243	71	9.243	77
10000.00	11.008	83	12.868	-21	.352	72	9.778	77
10500.00	12.294	88	12.667	-17	.485	78	10.799	83
11000.00	13.561	83	12.605	-19	.623	80	11.858	79
11500.00	13.541	82	11.626	-16	.744	83	11.447	78
12000.00	14.563	82	13.626	-4	1.127	97	12.172	79
12500.00	14.151	76	24.889	-18	2.602	81	11.738	74
13000.00	14.831	81	14.517	-46	2.056	52	12.232	81
13500.00	15.948	79	12.729	-32	2.772	50	13.332	79
14000.00	14.835	77	12.370	-35	2.562	6	12.370	70

REF PLANE EXT(CM): IN= 2.70, OUT= 2.70

PAGE 3: ANA*A5209/DEPT 0810 1/14/00
VARIAN METROLOGY LAB/C. NISHIMOTO
MBE FETS INGAAS

.00 VOLTS, .00 MA (MEAS 1) 46-5 VD-3.5V

FREQ (MHZ)	GA MAX DB	GU MAX DB	S21 DB	S12 DB	K MAG	U MAG
2000.000			.03	-30.88	.74	1.29
2500.000		15.06	-.17	-29.72	.91	.86
3000.000	11.79	12.88	-.40	-29.10	1.18	.54
3500.000	10.71	11.96	-.42	-29.07	1.37	.43
4000.000	9.32	10.39	-.52	-29.02	1.72	.29
4500.000	9.54	10.71	-.44	-29.05	1.67	.31
5000.000	9.08	10.23	-.48	-29.40	1.87	.26
5500.000	8.56	9.58	-.60	-29.87	2.15	.21
6000.000	8.61	9.61	-.58	-30.51	2.28	.20
6500.000	7.43	8.17	-1.03	-31.67	3.16	.12
7000.000	7.08	7.67	-1.36	-34.12	4.32	.09
7500.000	6.79	7.27	-1.44	-35.82	5.53	.06
8000.000	6.67	7.05	-1.41	-37.66	7.03	.05
8500.000	6.10	6.39	-1.69	-38.76	8.78	.04
9000.000	5.72	5.88	-1.79	-39.24	10.01	.03
9500.000	5.33	5.42	-1.94	-37.02	8.35	.03
10000.00	5.20	5.22	-2.21	-33.99	5.91	.05
10500.00	8.14	7.96	-1.79	-31.28	2.40	.14
11000.00	4.68	4.61	-2.81	-29.82	3.88	.07
11500.00	3.60	3.55	-3.30	-28.25	3.92	.07
12000.00	3.87	4.04	-2.37	-24.91	2.84	.10
12500.00		10.27	2.74	-17.88	.44	.57
13000.00	8.74	5.15	-1.92	-21.91	1.04	.18
13500.00	5.77	3.82	-3.33	-21.68	1.32	.16
14000.00	3.93	1.88	-4.84	-17.89	1.18	.18

REF PLANE EXT(CM): IN= 2.70, OUT= 2.70

VARIAN METROLOGY LAB/C. NISHIMOTO
MBE FETS INGAAS

.00 VOLTS, .00 MA (MEAS 1) 46-5 VD-3.5V

FREQ (MHZ)	Y11 MAG	Y11 ANG	Y21 MAG	Y21 ANG	Y12 MAG	Y12 ANG	Y22 MAG	Y22 ANG
2000.000	2.839	84	11.093	-8	.316	-113	2.699	60
2500.000	3.467	82	11.103	-9	.370	-116	3.168	62
3000.000	4.075	80	11.158	-11	.410	-120	3.653	61
3500.000	4.757	80	11.415	-12	.422	-123	4.164	62
4000.000	5.568	78	11.737	-14	.441	-125	4.740	62
4500.000	6.241	80	11.968	-15	.444	-127	5.221	65
5000.000	7.023	80	12.224	-16	.437	-130	5.756	66
5500.000	7.930	80	12.480	-17	.429	-132	6.415	67
6000.000	9.002	81	12.879	-18	.411	-135	7.148	69
6500.000	9.934	79	12.895	-20	.379	-140	7.941	69
7000.000	10.616	79	12.695	-21	.292	-149	8.178	69
7500.000	11.065	78	12.867	-22	.246	-154	8.489	69
8000.000	11.724	77	13.258	-23	.204	-165	8.833	69
8500.000	12.786	76	13.440	-23	.188	169	9.468	70
9000.000	13.725	75	13.893	-25	.186	138	9.999	69
9500.000	14.444	74	14.160	-28	.249	118	10.461	69
10000.00	15.385	75	14.148	-28	.365	105	10.967	69
10500.00	17.207	79	14.947	-26	.501	100	11.954	75
11000.00	18.680	74	15.041	-29	.671	93	13.134	71
11500.00	18.732	72	14.398	-28	.815	92	12.884	70
12000.00	20.088	71	17.055	-19	1.273	100	13.791	69
12500.00	20.439	67	30.516	-32	2.843	80	14.040	65
13000.00	20.394	70	18.442	-61	1.846	50	13.795	69
13500.00	21.297	69	15.936	-55	1.925	63	13.999	70
14000.00	22.778	65	14.741	-49	3.281	64	15.658	70

REF PLANE EXT(CM): IN= 2.70, OUT= 2.70

VARIAN METROLOGY LAB/C. NISHIMOTO
MBE FETS INGAAS

.00 VOLTS, .00 MA (MEAS 1) L6.4-1 VD=3V VG=-.5V

FREQ (MHZ)	GA MAX DB	GU MAX DB	S21 DB	S12 DB	K MAG	U MAG
2000.000	1.67	1.67	-6.21	-33.18	7.63	.00
2500.000	1.36	1.36	-6.25	-32.32	7.39	.00
3000.000	.87	.87	-6.25	-31.15	7.22	.00
3500.000	.53	.53	-6.25	-29.40	6.40	.00
4000.000	.11	.11	-6.20	-29.22	6.94	.00
4500.000	.83	.82	-6.06	-28.36	5.42	.00
5000.000	.85	.83	-5.97	-27.79	5.12	.00
5500.000	-.18	-.20	-6.09	-26.95	5.80	.00
6000.000	.31	.28	-5.98	-26.64	5.87	.00
6500.000	.08	.03	-6.10	-25.70	4.75	.00
7000.000	-.39	-.44	-6.18	-25.20	4.93	.00
7500.000	-.71	-.73	-6.34	-26.32	5.92	.00
8000.000	-.40	-.43	-6.23	-25.48	5.08	.00
8500.000	-.36	-.39	-6.12	-25.01	4.83	.00
9000.000	-1.76	-1.79	-6.69	-25.14	6.31	.00
9500.000	-2.05	-2.09	-6.75	-24.75	6.41	.00
10000.00	-1.48	-1.51	-6.60	-25.24	6.06	.00
10500.00	1.24	1.14	-6.28	-25.39	3.47	.00
11000.00	-1.34	-1.35	-6.55	-26.90	7.12	.00
11500.00	-2.21	-2.22	-6.78	-25.60	7.38	.00
12000.00	-2.62	-2.61	-6.78	-27.83	10.35	.00
12500.00	.99	1.01	-3.66	-30.91	9.20	.00
13000.00	-1.69	-1.70	-6.73	-39.01	30.32	.00
13500.00	-3.39	-3.41	-7.02	-33.73	23.64	.00
14000.00	-2.23	-2.45	-6.17	-13.98	2.17	.02

REF PLANE EXT(CM): IN= 2.70, OUT= 2.70

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VARIAN METROLOGY LAB/C. NISHIMOTO

MBE FETS INGAAS

.00 VOLTS, .00 MA (MEAS 1) L6.4-1 VD=3V VG=-.5V

FREQ	Y11		Y21		Y12		Y22	
(MHZ)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
2000.000	2.234	69	9.986	-14	.448	-131	18.897	-3
2500.000	2.681	71	10.026	-16	.499	-121	19.017	-4
3000.000	3.174	72	10.174	-20	.579	-115	19.216	-5
3500.000	3.770	73	10.292	-23	.716	-112	19.254	-5
4000.000	4.418	73	10.584	-26	.748	-110	19.619	-5
4500.000	5.084	78	10.809	-27	.830	-105	19.306	-5
5000.000	5.845	79	11.098	-30	.900	-102	19.994	-4
5500.000	6.944	78	11.247	-33	1.018	-103	19.833	-4
6000.000	7.277	79	11.489	-35	1.065	-97	20.167	-2
6500.000	8.454	80	11.643	-36	1.219	-95	20.348	-1
7000.000	8.967	79	11.730	-40	1.313	-88	20.336	-0
7500.000	9.286	79	11.322	-42	1.135	-103	19.379	-1
8000.000	10.019	81	11.604	-44	1.265	-93	19.353	-1
8500.000	11.184	81	12.030	-46	1.368	-92	19.250	0
9000.000	11.947	79	11.755	-48	1.405	-94	19.621	1
9500.000	12.711	78	12.391	-49	1.559	-100	21.095	1
10000.00	12.728	80	12.261	-50	1.434	-89	20.342	-3
10500.00	14.723	85	12.855	-47	1.423	-101	20.408	1
11000.00	16.070	81	12.938	-53	1.242	-96	19.277	1
11500.00	16.275	79	12.597	-53	1.442	-96	18.417	1
12000.00	16.295	77	12.325	-53	1.092	-114	17.344	2
12500.00	17.456	79	17.640	-56	.766	-137	16.959	7
13000.00	18.352	79	12.580	-71	.306	22	16.956	11
13500.00	18.183	73	12.333	-65	.569	13	16.133	10
14000.00	15.050	75	14.899	-79	6.063	-32	20.712	-1

REF PLANE EXT(CM): IN= 2.70, OUT= 2.70

VARIAN METROLOGY LAB/C. NISHIMOTO
MBE FETS INGAAS

.00 VOLTS, .00 MA (MEAS 1) L6.4-2 VD=3V VG= -.5V

FREQ (MHZ)	GA MAX DB	GU MAX DB	S21 DB	S12 DB	K MAG	U MAG
2000.000	.62	.79	-2.61	-26.58	6.89	.02
2500.000	.51	.68	-2.65	-26.54	6.98	.02
3000.000	.33	.48	-2.71	-26.46	7.17	.02
3500.000	.29	.43	-2.67	-26.41	7.23	.02
4000.000	.17	.30	-2.62	-26.21	7.30	.02
4500.000	.38	.52	-2.47	-25.86	6.80	.02
5000.000	.43	.55	-2.41	-26.06	6.94	.02
5500.000	.43	.55	-2.39	-25.98	6.88	.02
6000.000	.55	.67	-2.31	-25.87	6.67	.02
6500.000	.25	.35	-2.52	-26.15	7.20	.02
7000.000	.15	.24	-2.72	-26.49	7.49	.02
7500.000	.18	.28	-2.69	-26.63	7.57	.02
8000.000	.18	.27	-2.65	-26.75	7.72	.02
8500.000	.07	.15	-2.64	-26.55	7.74	.02
9000.000	-.04	.04	-2.66	-26.85	8.21	.02
9500.000	-.16	-.09	-2.73	-28.04	9.58	.01
10000.00	-.25	-.19	-2.89	-29.55	11.43	.01
10500.00	.38	.43	-2.66	-30.28	11.04	.01
11000.00	-.47	-.43	-3.19	-31.42	14.41	.01
11500.00	-.80	-.76	-3.50	-33.26	18.47	.01
12000.00	.04	.07	-2.72	-33.43	17.00	.01
12500.00	4.50	4.63	1.82	-30.70	7.54	.02
13000.00	.69	.73	-2.48	-33.32	14.88	.01
13500.00	-.45	-.43	-4.02	-29.45	10.38	.02
14000.00	-2.69	-2.77	-6.85	-22.22	5.49	.03

REF PLANE EXT(CM): IN= 2.70, OUT= 2.70

VARIAN METROLOGY LAB/C. NISHIMOTO
MBE FETS INGAAS

.00 VOLTS, .00 MA (MEAS 1) L6.4-2 VD=3V VG=-.5V

FREQ (MHZ)	Y11 MAG	Y11 ANG	Y21 MAG	Y21 ANG	Y12 MAG	Y12 ANG	Y22 MAG	Y22 ANG
2000.000	4.511	26	12.188	-9	.772	-161	7.024	12
2500.000	4.812	31	12.249	-11	.783	-157	7.175	14
3000.000	5.167	34	12.389	-14	.804	-154	7.452	16
3500.000	5.594	37	12.631	-16	.821	-150	7.695	18
4000.000	6.130	40	13.019	-19	.862	-146	8.066	21
4500.000	6.533	44	13.329	-20	.902	-142	8.307	25
5000.000	7.039	47	13.599	-22	.893	-140	8.549	27
5500.000	7.704	50	13.904	-23	.920	-136	8.958	31
6000.000	8.455	53	14.304	-25	.950	-133	9.429	35
6500.000	9.278	54	14.422	-27	.949	-132	9.988	37
7000.000	9.699	56	14.180	-29	.918	-130	10.157	40
7500.000	10.052	56	14.330	-31	.911	-127	10.234	41
8000.000	10.655	56	14.700	-33	.917	-125	10.553	43
8500.000	11.440	57	15.289	-34	.975	-125	11.120	42
9000.000	12.232	58	15.745	-37	.972	-131	11.622	44
9500.000	12.960	57	16.070	-40	.872	-130	12.024	45
10000.00	13.831	57	16.224	-41	.753	-131	12.526	47
10500.00	15.150	61	17.049	-40	.709	-123	13.247	52
11000.00	15.975	58	16.990	-43	.659	-128	14.035	51
11500.00	16.024	57	16.287	-44	.530	-128	13.618	50
12000.00	16.785	57	18.235	-37	.531	-125	13.897	52
12500.00	17.718	59	31.294	-49	.740	-156	14.383	55
13000.00	18.252	58	19.042	-77	.547	149	14.385	55
13500.00	18.842	59	15.947	-72	.853	122	14.567	58
14000.00	21.183	60	12.366	-70	2.107	96	15.977	61

REF PLANE EXT(CM): IN= 2.70, OUT= 2.70

VARIAN METROLOGY LAB/C. NISHIMOTO
MBE FETS INGAAS

.00 VOLTS, .00 MA (MEAS 1) L6.4-3 VD=3V VG=-.5V

FREQ (MHZ)	GA MAX DB	GU MAX DB	S21 DB	S12 DB	K MAG	U MAG
2000.000	-.78	-.78	-7.83	-33.16	11.07	.00
2500.000	-1.14	-1.14	-7.88	-31.64	10.05	.00
3000.000	-1.58	-1.57	-7.87	-30.38	9.62	.00
3500.000	-1.74	-1.74	-7.84	-29.16	8.72	.00
4000.000	-2.16	-2.15	-7.77	-28.25	8.70	.00
4500.000	-1.60	-1.59	-7.62	-27.26	6.97	.00
5000.000	-1.52	-1.52	-7.50	-26.55	6.40	.00
5500.000	-1.55	-1.55	-7.44	-25.80	5.96	.00
6000.000	-1.26	-1.28	-7.33	-25.18	5.27	.00
6500.000	-1.87	-1.88	-7.43	-24.88	5.78	.00
7000.000	-1.96	-1.97	-7.51	-24.53	5.61	.00
7500.000	-2.15	-2.15	-7.54	-24.19	5.62	.00
8000.000	-2.19	-2.19	-7.55	-23.74	5.39	.00
8500.000	-1.84	-1.84	-7.24	-23.39	4.95	.00
9000.000	-2.23	-2.22	-7.34	-23.32	5.31	.00
9500.000	-2.51	-2.50	-7.40	-23.45	5.70	.00
10000.00	-2.60	-2.59	-7.37	-23.52	5.88	.00
10500.00	-.10	-.12	-6.94	-23.08	3.36	.01
11000.00	-2.56	-2.55	-7.50	-23.91	6.01	.00
11500.00	-2.95	-2.91	-7.67	-24.57	6.94	.01
12000.00	-2.85	-2.80	-7.48	-23.86	6.40	.01
12500.00	-.19	-.12	-4.65	-19.62	3.01	.02
13000.00	-2.42	-2.39	-7.53	-25.96	7.31	.01
13500.00	-3.68	-3.67	-9.27	-27.69	9.75	.01
14000.00	-6.92	-7.01	-12.47	-22.98	8.27	.01

REF PLANE EXT(CM): IN= 2.70, OUT= 2.70

VARIAN METROLOGY LAB/C. NISHIMOTO
MBE FETS INGAAS

.00 VOLTS, .00 MA (MEAS 1) L6.4-3 VD=3V VG=-.5V

FREQ (MHZ)	Y11 MAG	Y11 ANG	Y21 MAG	Y21 ANG	Y12 MAG	Y12 ANG	Y22 MAG	Y22 ANG
2000.000	2.393	64	8.574	-14	.464	-117	19.795	-4
2500.000	2.809	66	8.604	-17	.558	-111	19.911	-5
3000.000	3.251	67	8.711	-21	.653	-108	19.986	-6
3500.000	3.752	69	8.824	-24	.758	-106	20.059	-6
4000.000	4.391	69	9.045	-28	.856	-104	20.143	-7
4500.000	4.910	74	9.225	-30	.961	-102	20.275	-8
5000.000	5.556	75	9.472	-33	1.056	-101	20.418	-8
5500.000	6.347	77	9.651	-35	1.166	-98	20.358	-7
6000.000	7.261	79	9.918	-37	1.271	-97	20.446	-6
6500.000	8.156	78	10.037	-40	1.345	-96	20.388	-5
7000.000	8.739	79	9.926	-43	1.399	-95	19.900	-5
7500.000	9.141	79	9.821	-45	1.445	-95	19.197	-5
8000.000	9.700	79	9.873	-48	1.531	-94	18.993	-6
8500.000	10.577	80	10.292	-49	1.604	-95	18.541	-6
9000.000	11.410	79	10.402	-52	1.652	-97	18.469	-6
9500.000	12.061	79	10.503	-55	1.656	-98	18.392	-7
10000.00	12.753	79	10.692	-55	1.666	-94	18.201	-6
10500.00	13.999	85	11.067	-56	1.726	-99	17.948	-5
11000.00	15.331	80	10.894	-61	1.647	-102	17.379	-4
11500.00	15.194	79	10.309	-62	1.473	-102	16.042	-4
12000.00	15.757	79	10.494	-62	1.591	-98	15.241	-4
12500.00	16.936	81	14.708	-69	2.626	-118	14.672	0
13000.00	17.299	80	10.188	-89	1.221	-160	13.918	2
13500.00	17.910	80	8.075	-89	.968	174	12.548	6
14000.00	19.357	78	5.652	-94	1.685	119	11.670	14

REF PLANE EXT(CM): IN= 2.70, OUT= 2.70

VARIAN METROLOGY LAB/C. NISHIMOTO
MBE & INP/INC FETS

.00 VOLTS, .00 MA (MEAS 1) 35.8-2 VD=2.3V VG=-3

FREQ (MHZ)	GA MAX DB	GU MAX DB	S21 DB	S12 DB	K MAG	U MAG
2000.000	14.65	15.20	1.26	-41.67	2.51	.17
2500.000	13.52	13.88	1.21	-40.04	2.66	.15
3000.000	13.25	13.50	1.23	-39.48	2.64	.14
3500.000	13.38	13.52	1.29	-38.30	2.30	.16
4000.000	12.54	12.62	1.40	-37.54	2.57	.14
4500.000	15.64	14.99	1.30	-38.28	1.49	.26
5000.000	14.36	13.90	1.41	-38.05	1.87	.19
5500.000	13.55	13.07	1.43	-37.97	2.18	.15
6000.000	13.23	12.74	1.48	-38.03	2.36	.13
6500.000	12.57	12.15	1.38	-38.25	2.74	.11
7000.000	12.57	12.11	1.29	-39.79	3.22	.09
7500.000	11.99	11.50	1.28	-40.79	4.07	.07
8000.000	11.19	10.70	1.02	-41.20	4.96	.06
8500.000	11.15	10.50	.74	-39.99	4.23	.06
9000.000	10.94	10.32	.71	-39.63	4.24	.06
9500.000	11.01	10.29	.62	-36.85	3.05	.09
10000.00	11.76	10.59	.46	-33.52	1.82	.15
10500.00	11.84	10.48	.45	-31.65	1.51	.17
11000.00		11.62	.38	-29.23	.76	.32
11500.00		13.10	.39	-27.25	.31	.59
12000.00		11.75	-.28	-25.45	.37	.58
12500.00		10.45	-.95	-23.28	.43	.59
13000.00			-1.19	-19.96	.15	1.17
13500.00			-1.68	-15.39	.06	1.25
14000.00		5.76	-.60	-15.58	.36	.32

REF PLANE EXT(CM): IN= 2.70, OUT= 2.70

#2

PAGE 2: ANA=A5209/DEPT 0810 4/28/88
VARIAN METROLOGY LAB/C. NISHIMOTO
MBE & INP/INC FETS

.00 VOLTS, .00 MA (MEAS 1) 35.8-2 VD=2.3V VG=-3

FREQ (MHZ)	Y11 MAG	Y11 ANG	Y21 MAG	Y21 ANG	Y12 MAG	Y12 ANG	Y22 MAG	Y22 ANG
2000.000	1.856	76	13.604	-4	.097	-119	2.969	16
2500.000	2.267	75	13.733	-6	.119	-112	3.173	19
3000.000	2.706	76	13.891	-7	.129	-106	3.341	23
3500.000	3.194	78	14.058	-7	.147	-100	3.478	27
4000.000	3.841	77	14.553	-9	.164	-96	3.808	31
4500.000	4.317	80	13.697	-6	.144	-86	4.235	64
5000.000	4.898	81	14.395	-7	.153	-83	4.558	56
5500.000	5.651	81	14.887	-8	.159	-77	5.048	55
6000.000	6.240	81	15.325	-9	.162	-73	5.353	53
6500.000	6.974	82	15.587	-11	.163	-70	5.685	51
7000.000	7.579	82	15.661	-11	.138	-62	6.141	54
7500.000	8.286	82	16.095	-13	.127	-43	6.516	54
8000.000	8.961	81	16.073	-15	.124	-24	6.939	54
8500.000	9.534	81	15.906	-14	.146	4	7.642	57
9000.000	10.227	81	16.186	-15	.156	19	7.817	57
9500.000	10.827	81	16.309	-15	.218	44	8.245	58
10000.00	11.589	82	16.288	-14	.326	55	8.984	62
10500.00	12.305	82	16.800	-15	.417	62	9.329	60
11000.00	12.904	83	16.488	-15	.545	67	9.334	63
11500.00	13.687	85	16.653	-16	.691	70	9.929	66
12000.00	14.687	83	16.037	-17	.884	74	10.757	69
12500.00	14.912	82	15.130	-15	1.157	78	11.264	70
13000.00	15.133	83	14.596	-14	1.682	78	11.411	70
13500.00	16.202	78	14.909	-9	3.075	60	12.435	67
14000.00	12.695	70	17.256	-23	3.076	-23	9.390	45

REF PLANE EXT(CM): IN= 2.70, OUT= 2.70

VARIAN METROLOGY LAB/C. NISHIMOTO
MBE & INP/ING FETS

.00 VOLTS, .00 MA (MEAS 1) 35.8-3 VD=2.3V VG-3V

FREQ (MHZ)	GA MAX DB	GU MAX DB	S21 DB	S12 DB	K MAG	U MAG
2000.000			3.77	-42.41	.91	1.32
2500.000	19.38	19.97	3.68	-40.38	1.21	.53
3000.000	19.42	19.43	3.71	-39.08	1.10	.54
3500.000	16.76	16.87	3.60	-37.62	1.42	.33
4000.000	14.82	14.97	3.68	-36.68	1.84	.22
4500.000			3.73	-37.55	.27	4.83
5000.000		21.45	3.74	-38.33	.53	.94
5500.000		19.48	3.71	-38.31	.69	.58
6000.000	19.29	17.48	3.62	-38.56	1.09	.35
6500.000	15.87	15.33	3.40	-39.04	1.86	.19
7000.000	15.34	14.82	3.16	-40.88	2.42	.14
7500.000	13.25	13.09	3.03	-43.79	5.23	.06
8000.000	12.40	12.11	2.71	-47.19	9.02	.03
8500.000	14.74	13.60	2.45	-40.76	2.54	.11
9000.000	14.07	12.94	2.33	-38.90	2.37	.12
9500.000	13.62	12.51	2.31	-37.11	2.16	.13
10000.00	14.65	12.74	2.21	-34.12	1.35	.20
10500.00	15.97	12.94	2.31	-32.42	1.06	.25
11000.00		14.02	2.23	-30.01	.53	.46
11500.00		15.22	2.20	-27.66	.17	.83
12000.00		14.09	1.57	-26.17	.20	.80
12500.00		12.68	.88	-24.34	.27	.75
13000.00			.69	-22.14	.00	1.27
13500.00			.41	-19.96	-.09	1.69
14000.00			-.06	-16.00	-.10	2.37

REF PLANE EXT(CM): IN= 2.70, OUT= 2.70

PAGE 2: ANA=A5209/DEPT 0810 4/28/88

VARIAN METROLOGY LAB/C. NISHIMOTO

MBE & INP/INC FETS

.00 VOLTS, .00 MA (MEAS 1) 35.8-3 VD=2.3V VG-3V

FREQ (MHZ)	Y11 MAG	Y11 ANG	Y21 MAG	Y21 ANG	Y12 MAG	Y12 ANG	Y22 MAG	Y22 ANG
2000.000	1.802	66	16.366	-3	.080	-126	2.117	83
2500.000	2.170	67	16.768	-4	.105	-115	2.615	74
3000.000	2.572	68	17.011	-6	.125	-108	3.140	76
3500.000	3.106	70	17.467	-6	.152	-104	3.723	69
4000.000	3.586	69	18.206	-8	.178	-102	4.245	63
4500.000	4.038	74	17.130	-7	.148	-96	5.112	89
5000.000	4.513	75	17.684	-7	.139	-89	5.672	86
5500.000	5.222	76	18.199	-8	.144	-84	6.372	84
6000.000	5.845	76	18.622	-9	.145	-81	6.890	81
6500.000	6.629	76	19.014	-10	.144	-80	7.343	77
7000.000	7.280	76	18.987	-10	.120	-71	7.940	78
7500.000	7.899	74	19.597	-14	.089	-73	8.371	75
8000.000	7.965	72	19.380	-15	.062	-18	8.763	74
8500.000	8.553	75	18.671	-13	.129	32	9.678	79
9000.000	9.155	76	18.937	-14	.164	41	10.012	77
9500.000	9.675	76	19.322	-14	.206	49	10.182	75
10000.00	10.353	77	19.546	-13	.298	57	10.944	76
10500.00	11.004	78	20.110	-14	.369	64	11.156	76
11000.00	11.593	79	19.949	-14	.488	70	11.649	78
11500.00	12.295	81	20.140	-16	.647	72	12.330	79
12000.00	13.271	80	19.605	-18	.804	74	12.968	78
12500.00	13.637	79	18.544	-17	1.016	76	13.164	77
13000.00	13.521	80	17.815	-18	1.285	71	13.035	78
13500.00	13.701	79	17.256	-18	1.654	70	12.907	77
14000.00	15.220	77	17.511	-13	2.793	65	13.902	75

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